



MOS Integrated Circuit

μ PD61210/12

EMMA2SL – SECOND GENERATION ENHANCED MULTIMEDIA ARCHITECTURE PROCESSOR FOR DIGITAL TV RECEIVERS / DECODERS

DESCRIPTION

The μ PD6121x devices, EMMA2SL, are members of the second generation of multimedia processors based on NEC's Enhanced MultiMedia Architecture (EMMA™). These devices provide nearly all the functionality required to realise a high performance and cost-effective digital set-top box or integrated digital TV.

FEATURES

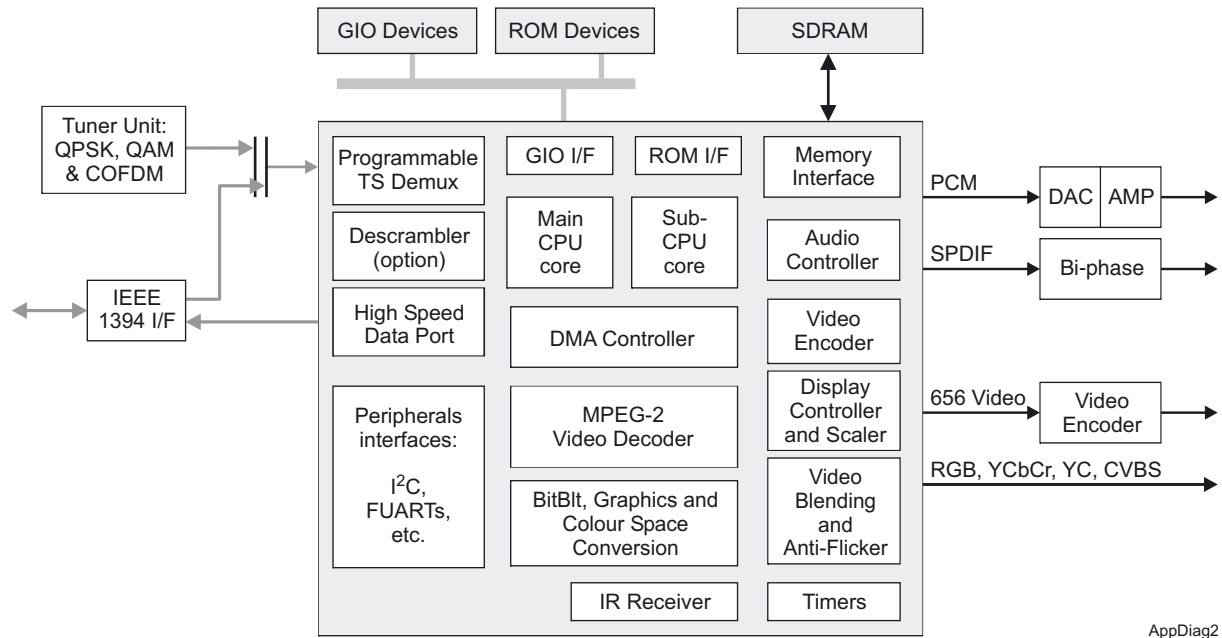
- ◆ MPEG1 and MPEG2-TS/PS compliant
- ◆ High performance MIPS32™ 4KEc™ main CPU core
- ◆ High performance MIPS32™ 4KEm™ sub-CPU core
- ◆ Integrated DVB descrambling with family options for Irdeto
- ◆ 36 PID filters, 32 section filters
- ◆ Video Outputs: 4 DACs for RGB, component video, S-video and composite output with support for PAL, NTSC and SECAM
- ◆ 5 graphics planes
- ◆ Support for Macrovision™ analog video copy protection (μ PD61212 only)
- ◆ Audio Output: 2-channel PCM and SPDIF
- ◆ Peripherals support:
 - two fast UARTs with 16byte FIFOs
 - two I²C interfaces
 - two Smart Card interfaces
 - infrared receiver
 - three wire clocked serial interface
- ◆ System timers, RTC and Watchdog timer
- ◆ Motorola/Intel Bus.

ORDERING INFORMATION

Part Number	Description	Remarks
μ PD61210 GM-100-GAA-A	Standard part – Pb free	
μ PD61212 GM-104-GAA-A	With Macrovision support – Pb free	Please contact NEC for details of the CA/descrambler variants.

The information in this document is subject to change without notice.
Before using this document, please confirm that this is the latest version.
Not all devices/types are available in every country. Please check with the local NEC representative for availability and additional information.

TYPICAL APPLICATION



FEATURE LIST

Main Processor

- ◆ High Performance MIPS32 4KEc CPU core
- ◆ 32bit RISC MIPS architecture
- ◆ Supports the MIPS-I, MIPS-II and a subset of the MIPS-III instruction sets
- ◆ 4KByte instruction cache, 4KByte data cache
- ◆ 2 way cache accessing
- ◆ EJTAG debug support

Sub-Processor

- ◆ High Performance MIPS32 4KEc CPU core for audio MPEG decoding
- ◆ 4KByte instruction cache, 4KByte data cache
- ◆ 8KByte scratch-pad memory support

Unified Memory Interface

- ◆ Supports 16bit bus width SDRAM
- ◆ Unified CPU/MPEG/Graphics memory
- ◆ Supports data rates up to 133MHz
- ◆ Supports 8, 16, 32 or 64Mbytes total memory

ROM/GIO Interface

- ◆ Total address area 64Mbyte for ROM
- ◆ Supports normal, page and flash ROM
- ◆ Supports NOR and NAND flash ROM
- ◆ 2 chip select signals for ROM
- ◆ 8MByte total address area for GIO
- ◆ 2 chip select signals for GIO
- ◆ PCMCIA support (16-bit PC Card only)

DMA

- ◆ Supports DMA transfers to/from GIO and memory-to-memory

Programmable TS De-multiplexer

- ◆ Single stream input configurable as a parallel or serial port
- ◆ Supports MPEG2-TS

- ◆ Maximum input bit rate 100Mbit/sec
- ◆ High Speed Data port output for external IEEE1394 link devices
- ◆ 36 PID filters:
 - 1 Video PID
 - 2 Audio PIDs
 - 1 PCR PID
 - 32 general PIDs
- ◆ 32 section filters (8-Byte/16-byte depth)

Descrambler

- ◆ Supports decryption with 16 key-pairs

MPEG video decoder

- ◆ MPEG-2 MP@ML standard compliant
- ◆ Supports MPEG-1 and -2 elementary streams

Audio Processor

- ◆ MPEG-1 and -2, layer 1 and 2
- ◆ PCM L+R audio output
- ◆ SPDIF output
- ◆ Test-tone and Mixing

Graphics engine

- ◆ 2-D image data transfer
- ◆ Colour space conversion: RGB32 to YCbCr
- ◆ Colour expansion

Display

- ◆ 5 graphics planes: background colour, live video, still picture and two OSD planes
- ◆ 256-level alpha blending between all planes
- ◆ Real time scaler for the live video and still picture planes supporting independent horizontal and vertical scale factors between 8 and 1/4
- ◆ Anti-flicker filtering for OSD
- ◆ Independently blended output for VCR

Video Encoder

- ◆ 4 DACs for analog RGB, YCbCr/YPbPr, YC and CVBS video outputs
- ◆ PAL, NTSC and SECAM formats
- ◆ VBI insertion for Closed-Caption, Teletext, Video-ID, WSS, VPS and CGMS
- ◆ Support for Macrovision analog video copy protection (μPD61212 only)
- ◆ CCIR-656 digital output

Peripheral support

- ◆ Two asynchronous fast UARTs

- ◆ Clocked Serial Interface
- ◆ Two I²C compatible interface
- ◆ Infrared receiver interface
- ◆ Two Smart Card interfaces
- ◆ A timer supporting input capture and output compare
- ◆ A system timer, a real-time clock and a watch-dog timer
- ◆ Programmable Pin Port shared with other peripherals

Package

- ◆ 216-pin, 0.4mm pitch, QFP (Quad Flat Pack)

CONTENTS

1	FUNCTIONAL DESCRIPTION	7
1.1	Overview	7
1.2	Block Diagram	7
1.3	Processors	7
1.4	Memory Interfaces	8
1.4.1	Unified Memory Interface	8
1.4.2	ROM Interface	8
1.4.3	General IO Interface	8
1.5	Signal Processing	8
1.5.1	Programmable transport de-multiplexer	8
1.5.2	DMA controller	8
1.5.3	MPEG video decoder	8
1.5.4	Audio controller module	9
1.5.5	Graphics engine	9
1.5.6	Display module	9
1.5.7	Video encoder	9
1.6	Peripherals	9
1.7	Timers	10
1.8	Debugging	10
1.9	Configuration	10
1.10	VCXO Mode	10
2	PIN CONFIGURATION	11
2.1	Overview	11
2.2	Boot Configuration	12
2.2.1	Boot mode	12
2.2.2	Strap Pin Settings	12
2.3	Functions and Interfaces with Dedicated Pins	14
2.4	Interfaces which Share Pins	17
2.4.1	Optional Interface Numbering	17
2.4.2	Boot Modes	17
2.4.3	Default Interface Numbering	18
2.4.4	Shared Interface Conflicts	18
2.4.5	Optional Interface Pin Arrangements	19
2.5	Pin Identification	28
3	ELECTRICAL SPECIFICATIONS	31
3.1	Absolute Maximum Ratings	31
3.2	Recommended Operating Range	31
3.2.1	Power-on sequence	31
3.3	DC Characteristics – General	31
3.4	DC Characteristics – Unified Memory Interface	32
3.5	DC Characteristics – I ² C Interface	32
3.6	DAC Characteristics – Analog Video Outputs	32
3.6.1	NTSC – Composite output	33
3.6.2	NTSC – Y/C output	33
3.6.3	NTSC – Y/Pb/Pr output	34

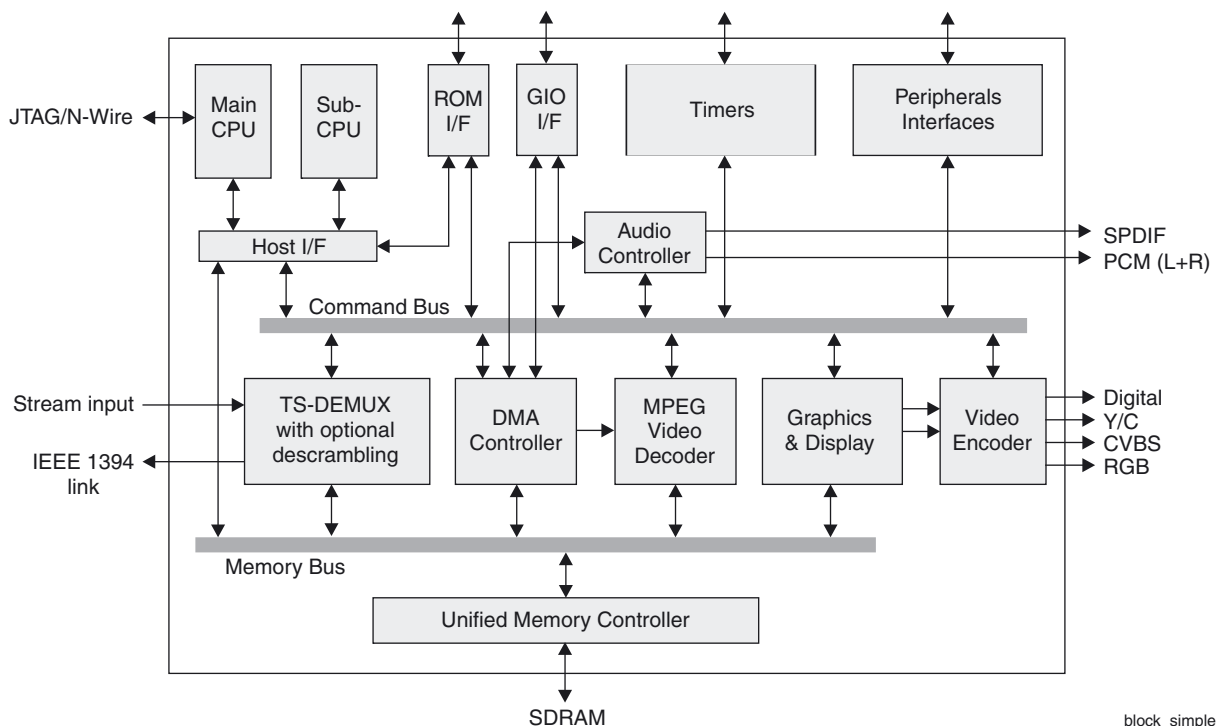
3.6.4	NTSC – RGB output	35
3.6.5	PAL – Composite output	35
3.6.6	PAL – Y/C output	36
3.6.7	PAL – Y/Pb/Pr output	36
3.6.8	PAL – RGB output	37
4	AC TIMING SPECIFICATIONS	38
4.1	System	38
4.1.1	27MHz Clock	38
4.1.2	Reset and Strap Input Timing.	38
4.2	Unified Memory Interface	39
4.3	ROM Interface	39
4.3.1	NOR Flash ROM	39
4.3.2	NAND Flash ROM	41
4.4	General IO Interface	45
4.4.1	Motorola and Intel Modes.	45
4.4.2	GIO Configured as a PCMCIA Interface	50
4.5	Stream Interface	54
4.5.1	Parallel configuration	54
4.5.2	Serial configuration	55
4.6	Video Output – Digital.	55
4.7	High Speed Data Interface	56
4.8	Audio Outputs.	57
4.8.1	PCM Output Timing.	57
4.8.2	SPDIF Output Timing.	57
4.9	I ² C Interface.	58
4.10	Fast UART Interface	58
4.11	CSI (Clocked Serial Interface)	59
4.12	IR Receiver Interface	59
4.13	Smart Card Interface	60
4.14	VCXO Interface	60
5	PHYSICAL SPECIFICATIONS	61
5.1	Package Drawing: 216-pin Plastic LQFP (Fine Pitch) (24x24)	61
5.2	Soldering Conditions	61

1 FUNCTIONAL DESCRIPTION

1.1 Overview

The μ PD6121x devices integrate the functions of a programmable TS de-multiplexer, a DMA controller, an MPEG video decoder, a programmable audio controller, graphics and display engines, a video encoder and DACs, and various interfaces to support peripheral modules. The device has been designed with a memory interface using glueless logic supporting 16-bit bus width SDRAM. The μ PD6121x incorporates two processors, two main buses and a peripherals bus. Both processors are MIPS32 cores and both can access all modules within the device.

1.2 Block Diagram



1.3 Processors

The μ PD6121x devices have one MIPS32 4KEc core for the main CPU and one 4KEm core for the sub-CPU. These are high performance RISC CPUs. Overall system efficiency is promoted by the incorporation of on-chip 4KByte instruction and 4KByte data caches.

The main CPU is for running user programs and supports the entire MIPS II instruction set plus MIPS III 32bit instructions for the MDU (Multiply Divide Unit), TLB (Translation Lookaside Buffer), MMU (Memory Management Unit) and MAC (Multiply Accumulate Unit).

The sub-CPU supports the MIPS II instruction set and incorporates an 8KByte scratch-pad memory. The primary function of the sub-CPU is audio decoding.

A dedicated ROM interface keeps the memory bus free during instruction fetches which helps to keep bus efficiency high for other bus masters. A unified memory architecture is used to minimise system memory costs. Development time is minimised by the provision of an enhanced JTAG (EJTAG) debugging interface.

1.4 Memory Interfaces

1.4.1 Unified Memory Interface

The unified memory controller supports SDRAM devices with a 16-bit bus width. Memory bandwidth is in the order of 250Mbytes/s at a bus speed of 133MHz. Memory modules can be 8, 16, 32 or 64Mbytes.

1.4.2 ROM Interface

The ROM interface supports most current types of ROM: normal, page and flash ROM. Flash ROM can be NOR or NAND flash. The total memory area can extend to 64Mbytes across 2 chip selects. Each chip select can be configured for 4, 8, 16 or 32Mbytes.

1.4.3 General IO Interface

The General IO module operates in single access mode. Single access mode transfers data to or from devices on the external GIO bus via the internal command bus (C-bus). The maximum address area supported is 8Mbytes with 2 chip selects.

The module supports endian exchange, an 8 or 16bit bus width, Motorola or Intel interface formats and PCMCIA master mode.

1.5 Signal Processing

The μ PD6121x incorporates a transport demultiplexer and filter block, a standard MP@ML MPEG-2 video decoder and a programmable audio controller supporting MPEG-1 and 2 at level 1 and 2. Decoded video data is handled by a 2-D BitBlit graphics engine, a display processor supporting 4 video planes and a video encoder with PAL, SECAM, NTSC and digital outputs.

1.5.1 Programmable transport de-multiplexer

The transport de-multiplexer processes MPEG-2 transport streams at a maximum data input rate of 100Mbits/s. The μ PD6121x can be configured with either a serial or parallel interface port. The module can also output stream data via a high speed data port to provide support for external IEEE1394 link devices.

The filtering block provides PID filtering for one Video, two Audio, one PCR and 32 general PIDs. There are also 32 section filters of 8Byte depth which can be arranged in pairs to provide 16Byte filtering.

The TS Demux block extracts the Program Clock Reference (PCR) field and provides a latched STC value at arrival time. This mechanism can be used to perform clock recovery and to control an external VCXO using the PWM output.

If a descrambler family option is incorporated, the filtered stream can then be passed through the chosen descrambler.

The data is output to circular buffers in unified memory from where it can be accessed by the main CPU, the MPEG video decoder and the sub-CPU for audio decoding.

1.5.2 DMA controller

The DMA controller is responsible for A/V code buffer management and transferring stream data to the MPEG video decoder. It also supports data transfers to/from the GIO and memory-to-memory transfers in the unified memory.

1.5.3 MPEG video decoder

MPEG video decoder handles standard main profile at main level MPEG-2 streams. It also accepts MPEG-1 and MPEG-2 elementary video streams. The module can be programmed to use various modes of error concealment.

1.5.4 Audio controller module

The audio controller handles layers 1 and 2 for MPEG-1 and -2 and can output stereo PCM and SPDIF with IEC60958 encoding. A test-tone generator and a mixing facility with separate left and right attenuation are also included.

1.5.5 Graphics engine

The graphics engine incorporates a 2-D bit-blitter with a colour space conversion function supporting the conversion of RGB32 format data to YCbCr 4:2:2 format. Colour space conversion may be used to support scaling of OSD data by using the real-time scaler for the still plane in the display module which only accepts YCbCr 4:2:2 or 4:2:0 format data. The graphics engine also supports colour expansion which may be used to increase the bit-depth of one or two bit font data.

1.5.6 Display module

The display module handles five planes: live video, still picture, OSD1, OSD2 and a background colour plane. The video plane is for decoded MPEG video. Full 256-level alpha blending between all five planes is supported and the display module also incorporates a capture function for grabbing live video frames.

There is a real-time scaler for the video plane supporting horizontal and vertical scale factors from 1/4 to 8 handling both 4:2:2 and 4:2:0 format data. Horizontal scaling uses a 7-tap filter. Vertical scaling uses a 5-tap filter for luma and a 3-tap filter for chroma.

The OSD planes support CLUT and RGB formats. CLUT modes are 1, 2, 4 and 8bpp; RGB modes are 12bpp plus 4bit alpha, 15 plus 1bit alpha, 16bpp and 32bpp. Anti-flicker filtering for the OSD planes is provided by a 3-tap filter.

1.5.7 Video encoder

The video encoder and sync generator modules support NTSC, PAL and SECAM video standards including PAL-M, PAL-N and PAL-Nc.

There are 4 DACs for analog video output providing for composite (CVBS), S-video (Y/C) and component video (RGB or YPbPr/YCbCr). A digital output compliant with Rec.656 is also available. The encoder includes a VBI data insertion function for Closed Captions, Teletext, WSS, VPS, CGMS and Video ID.

There are Brightness and Contrast functions for all analog video outputs.

Macrovision analog copy protection is available as a family option in the μ PD61212.

1.6 Peripherals

Peripherals are supported by:

- ◆ Two asynchronous 16550 compatible UARTs with 16Byte FIFOs.
- ◆ A 3-wire Clocked Serial Interface supporting operation stop mode and 3-wire serial I/O mode.
- ◆ Two multi-master, I²C compatible interfaces.
- ◆ Two Smart Card interfaces supporting ISO-7816, EMV and Mondex.
- ◆ An infrared receiver interface – an input capture timer that measures the interval between adjacent edges of the demodulated signal from an IR detector/amplifier.
- ◆ A general purpose, programmable pin interface of up to 45 pins.

These pins are shared with other peripherals. If more general purpose I/Os are needed than are left free after all required optional interfaces are enabled, it is possible to use spare ROM address pins with an external data latch such as a TTL 74574. Two sets of clock and enable signals are available to control such external latches.

1.7 Timers

There are a number of timers that can be used for various purposes.

Capture/compare timer This timer can be configured as either a capture or compare timer. In capture mode the timer can be used for timing signal edges on an input pin. In compare mode the timer can toggle an output pin at preset counter values. In both modes the timer has a resolution programmable from 0.217 μ s to 0.889ms and the 16bit free run counter allows a programmable period from 14.22 msec to 58.25 sec.

System timer This timer can be used for software timing. The resolution and period can be programmed within the same limits as the capture/compare timer. This timer generates an internal interrupt for the main and sub-CPU when the count reaches the preset value.

Real-time clock The real-time clock may be used to keep track of the time of day. Timer resolution is in the order of 1 ms. The real-time clock generates an internal interrupt at a preset value or when the counter wraps after 24 hours.

Watch dog timer This is used to detect hardware or software failures. This timer has a 12-bit prescaler to generate the counter clock and 16-bit free-run and programmable counters. The timeout is programmable from 222 μ s to 14.5s in 222 μ s steps. The watch dog timer generates a non-maskable interrupt for the CPU or the RSTOUT pin.

1.8 Debugging

The μ PD6121x supports a JTAG port with full boundary scan.

1.9 Configuration

ROM Boot options are determined by holding certain strap pins high during device initialisation. Other strap pins are used to define system options such as clock speeds, endian configuration and so on.

A number of functions of the μ PD6121x share pins. After initialisation, interface functions can be set dynamically using register settings.

1.10 VCXO Mode

The μ PD6121x supports both internal and external VCXOs. When using the internal VCXO an external 27MHz (\pm 50ppm) crystal is required. Otherwise an external 27MHz clock input must be connected.

2 PIN CONFIGURATION

2.1 Overview

The μPD6121x is designed for maximum flexibility of pin assignment with a minimum device cost.

There are five groups of pins on the device:

- 1 Power and ground
- 2 Strap pins – these are shared with other functions but act as strap pins at start-up
- 3 Dedicated interfaces – for functions that are always available
- 4 Default interfaces – for functions that are available by default but which share pins with optional interfaces
- 5 Optional interfaces.

Strap Pins

Boot mode and system configuration are set by strapping – holding certain pins high or low at system start-up or reset. The state of the strap pins (RADD0 – RADD23) at start-up decides the configuration of the following:

- ◆ processor clock speed
- ◆ processor endian mode
- ◆ processor merge mode
- ◆ pin configuration for the enhanced JTAG interface
- ◆ memory clock speed
- ◆ ROM interface endian mode
- ◆ ROM type and area used for booting
- ◆ ROM bus width.

Dedicated Interfaces

The interfaces always available are:

- ◆ system pins (clock, reset, JTAG, etc.)
- ◆ unified memory
- ◆ PCM and SPDIF audio output
- ◆ both I²C interfaces
- ◆ fast UART1 TX and RX pins (*see also 'Optional interfaces' on page 12*)
- ◆ analog video out.

Default Interfaces

These interfaces are available at start-up but may lose some pins or be totally disabled if any optional interfaces are selected.

- ◆ ROM/GIO (*additional chip selects are available as an option*)
The ROM/GIO Interface block supports external ROM by default but can be configured to support NAND flash ROM, PCMCIA cards (not CardBus) and a General I/O (GIO) interface.
- ◆ PPORT (Programmable Pin Port)
Any pins of the Programmable Pin Port (PPORT0 – 44) not used by enabled interfaces may still be used as general purpose I/O pins. Each pin can be configured independently to be an input or output.

Optional interfaces

- ◆ one serial or one parallel TS input
- ◆ a High Speed Data output (HSD) for AV data
- ◆ two fast UARTs with FIFOs (*see Note*)
- ◆ two Smart Card interfaces
- ◆ a three-wire clocked serial interface
- ◆ an infrared interface input
- ◆ a digital video output
- ◆ the I/O port for the capture/compare timer.

Note

The TX and RX pins of fast UART1 are not shared and are available by default at start-up. The remaining modem control pins are enabled using interface option 14 or 15.

2.2 Boot Configuration

The μPD6121x can boot from either internal code stored in a ROM area within the ROM interface or from external ROM connected to the default ROM interface pins. The internal boot code is to support system initialisation from NAND flash ROM and to provide other boot options.

2.2.1 Boot mode

There are two boot modes:

A Normal boot mode using external NOR flash ROM.

B Boot from NAND Flash ROM. When this mode is selected the internal boot ROM sets up the ROM interface to support NAND flash ROM. The ROM data pins RDATA0 to RDATA7 are used for the NAND data bus and four ROM Address pins are used for NAND control signals.

2.2.2 Strap Pin Settings

The boot mode and system configuration are set using the strap pins listed in [table 1](#) below. The timing for these settings is shown in the [Reset and Strap Input Timing](#) diagram on [page 38](#).

All strap pins must be pulled either high or low at start-up.

Table 1 Start-up configuration pins

Pin Name	Pin Numbers	Function
RDATA0	15	Endian for main MIPS32 CPU
RDATA1~2	16, 17	Merge Mode for main MIPS32 CPU
RDATA3	18	<i>Reserved</i>
RDATA4~5	19, 20	VRCLK: main and sub-CPU clock
RDATA6~7	21, 22	MCLK: memory clock
RDATA8	23	Endian mode for ROM interface
RDATA9	24	ROM bus width
RDATA10	28	MINIBOOT
RDATA11~12	29, 30	BOOTSEL
RDATA13	31	EJTAG_MODE
RDATA14	32	DSYSELB
RDATA15	33	DINTEN
RADD21~22	59, 60	VCXO mode.

RDATA[0] Sets the endian mode for the main MIPS32 CPU.

- 0** Little Endian
- 1** Big Endian

RDATA[2:1] Sets the merge mode for the 16-byte collapsing write buffer for the MIPS32 4KEc main CPU. Refer to the MIPS32 4KEc Processor Core documentation for details.

- 00** No merge && ALL bytes enable
- 01** No-Merge && Simple bytes enable
- 10** Full merge && ALL bytes enable
- 11** Full merge && Simple bytes enable

RDATA[3] Reserved for testing purposes. This pin must be held low during reset.

RDATA[5:4] Sets the clock for the main and sub-CPU cores.

- 00** 127.008MHz
- 01** 162MHz
- 10** 165.888MHz
- 11** 186MHz

RDATA[7:6] SDRAM memory clock. This sets the clock frequency on the DCLK pin of the memory interface.

- 00** 126.9MHz
- 01** 132.75MHz
- 10** Reserved
- 11** Determined by the MCLK Divider Register

RDATA[8] ROM bus endian mode. The ROM bus can be configured to operate in either little or big endian mode to suit the connected ROM.

- 0** Little Endian
- 1** Big Endian

RDATA[9] ROM bus width mode and NAND flash ROM size. The purpose of this strap depends on the setting of RDATA[10].

For RDATA[10] = '0'

Selects the ROM BUS width:

- 0** 16 bit mode
- 1** 8 bit mode

For RDATA[10] = '1'

Selects NAND flash ROM size:

- 0** 256Mbit or less NAND flash
- 1** 512Mbit or more NAND flash

RDATA[10] Internal Boot ROM. Note that if this pin is set to '0' the RDATA[12:11] pins should also be set to '00'.

- 0** Boot from external NOR ROM (Boot mode A)
- 1** Boot initially from internal boot ROM (Boot mode B)

RDATA[12:11] Specifies the boot method used when the internal boot ROM is used. If Internal boot ROM is *not* used these pins must be pulled low at start-up.

- 00** Reserved
- 01** Reserved
- 10** Reserved
- 11** Mode B: boot from NAND flash ROM

RDATA[13] Enhanced JTAG (EJTAG) mode.

- 0** JTAG
- 1** EJTAG

RDATA[14] EJTAG Daisy-chain enable.

- 0** Main CPU → sub-CPU
- 1** Main CPU only

RDATA[15] DINTEN pin configuration for Enhanced EJTAG.

- 0** Disabled
- 1** Enabled

RADD[22:21] Sets the mode for the internal/external VCXO unit.

- 00** Enables the internal VCXO. PWMOUT pin does not output 27MHz clock.
- 10** Disables the internal VCXO. An external VCXO device must be used.
- 01, 11** Reserved.

2.3 Functions and Interfaces with Dedicated Pins

Tables 2 to 13 list all the functions that do not share pins.

Table 2 Unused pins

Pin name	Pin no.	Disposition
N/C	168	Connect to ground
N/C	170	Not connected
N/C	201	Connect to ground

Table 3 Test

Pin name	Pin no.	Description	In/Out
TEST	72	For test use only. Connect to GND.	I

Table 4 Power and Ground

Pin name	Pin nos.	Description
GND1	11, 42, 74, 141	Main supply ground
GND2	154, 162, 163, 176, 184, 193, 206, 214	
GND3	26, 54, 92, 110, 215	
DAGND03 DAGND02 DAGND1 DAGND12 DAGND13	75, 78, 83, 88, 91	Analog Ground for video DACs
PAGND	134, 138	Ground for PLL 1.5V supply
DAVDD02 DAVDD01 DAVDD11 DAVDD12	77, 80, 86, 89	3.3V supply for video DACs
VDD1	12, 43, 66, 73, 133, 177, 207	1.5V supply (core)
VDD2	155, 164, 175, 185, 194, 205, 213	3.3V for Unified Memory I/F IO buffers
VDD3	25, 27, 53, 93, 109, 142, 216	3.3V for IO buffers
PAVDD	135, 139	1.5V supply for PLL

Table 5 System

Pin name	Pin no.	Description	In/Out
CLK27IN	140	27MHz Input clock from VCXO	I
CLK27OUT	143 ^A	Internal VCXO Out	O
RSTOUT	144	RESET out from Watch Dog Timer	O
RSTSWB	145	Hardware RESET	I
NMI	146	Non Maskable Interrupt (see note A in table 7 below)	I

A Depending on the VCXO strap setting (see 'Strap Pin Settings' on [page 12](#)), pin 143 can be either CLK27OUT or PWMOUT, as shown in the following table.

Table 6 PCR

Pin name	Pin no.	Description	In/Out
PWMOUT	143	PWM output to control the 27MHz VCXO	O

Table 7 JTAG

Pin name	Pin no.	Description	In/Out
JTDI	149	EJTAG data input	I
JTCK	152	EJTAG clock	I
JTD0	150	EJTAG data output	O
JTMS	151	EJTAG mode select	I
JTRST	153	EJTAG reset	I
EDINT	146 ^A	Debug interrupt	I

A In normal use, pin 146 is exclusive to the NMI input. In debugging mode, pin 146 is the EDINT input.

Table 8 VCX

Pin name	Pin no.	Description	In/Out
XT1	137	Oscillator input	I
XT2	136	Oscillator output	O

Table 9 Unified Memory Interface

Pin name	Pin nos.	Description	In/Out
DADD0~DADD13	189 (DADD0), 188, 187, 186, 183, 182, 181, 180, 179, 178, 190, 174, 173, 200 (DADD13)	Address Bus	O
DQ0~DQ15	212 (DQ0), 211, 210, 209, 208, 204, 203, 202, 166, 165, 161, 160, 159, 158, 157, 156 (DQ15)	Data Bus	I/O
DCSB	195	Chip select	O
DRASB	196	RAS signal	O
DCASB	197	CAS signal	O
DWEB	198	Command write enable	O
DQM0~DQM1	199, 169	Data mask	O
DBA0~1	192, 191	Bank address	O
DCKE	172	Clock enable	O
DQS1	167	Connect to DCLK	I
DCLK	171	Clock output	O

Table 10 Audio Output

Pin name	Pin no.	Description	In/Out
AMCK	65	PCM Audio Master Clock	O
ALRCK	70	PCM Audio L/R Clock	O
ABCK	67	PCM Audio Data Clock	O
AD0	69	PCM Audio Data – L/R	O
ATX	68	SPDIF Digital audio output	O

Table 11 Video DAC outputs^A

Pin name	Pin no.	Description
VACVBS	79	Composite video (analog)
VAY	76	Y signal (analog)
VAPR	87	Pr signal
VAPB	90	Pb signal
RSET0	81	Resistor for adjusting full scale currents
RSET1	85	
REF0	82	External voltage reference
REF1	84	

A See also 'DAC Characteristics – Analog Video Outputs' on page 32.

Table 12 I²C Interfaces 0 and 1

Pin name	Pin no.	Description	In/Out
SDA0	114	I ² C-0 Serial Data	I/O
SCL0	115	I ² C-0 Serial Clock	I/O
SDA1	116	I ² C-1 Serial Data	I/O
SCL1	117	I ² C-1 Serial Clock	I/O

Table 13 Fast UART 1

Pin name	Pin no.	Description	In/Out
RXD1B	147	Receive data	I
TXD1B	148	Transmit data	O

The RXD1B and TXD1B pins in the UART1 interface are not shared, however, the remaining pins are shared and so the UART1 i/f is also listed in [table 29 on page 26](#) and [table 30](#).

2.4 Interfaces which Share Pins

This section describes both the default and optional interfaces which share pins.

2.4.1 Optional Interface Numbering

The optional interfaces are numbered as follows:

- | | |
|--|---|
| 0 PCMCIA interface (memory + I/O) | 11 3-wire clocked serial interface (CSI) |
| 1 PCMCIA interface (memory only) | 12 Extended ROM/GIO (extra chip select) |
| 2 <i>Reserved</i> | 13 Fast UART 0 |
| 3 Parallel TS input | 14 Fast UART 1a (standard pinning) |
| 4 Serial TS input | 15 Fast UART1b (alternate pinning) |
| 5 High Speed Data output (HSD) | 16 Infrared interface input (IR-in) |
| 6 <i>Reserved</i> | 17 <i>Reserved</i> |
| 7 Smart Card interface 0 (SCI0) | 18 Extended ROM address (3 pins) |
| 8 Smart Card interface 1 (SCI1) | 19 External data latch control 0 |
| 9 Digital video output | 20 External data latch control 1 |
| 10 Capture/Compare Timer port | 21 NAND Flash ROM |

2.4.2 Boot Modes

The boot mode affects interfaces as follows:

- A** Boot from external ROM: the ROM/GIO interface is used with its default ROM configuration.
- B** Boot initially from internal ROM then from external NAND flash ROM: the ROM/GIO interface is configured to support NAND ROM in the same way as enabling option 21 after start-up.

2.4.3 Default Interface Numbering

The default interfaces which share pins are numbered as follows:

D1 ROM/GIO

D2 PPORT pins 0 – 44

2.4.4 Shared Interface Conflicts

Following start-up, multiple interfaces can be enabled subject to the restrictions shown in [table 14](#) below.

Where there is a conflict the lower-numbered option generally has priority. For example, if the HSD output (option 5) is enabled by setting the appropriate register bit then there are three consequences:

- ◆ the fast UART1b modem control pins (option 15) cannot be enabled at the same time
- ◆ the Extended ROM address pins (option 18) cannot be enabled at the same time
- ◆ the default interface D2 is restricted – PPORT pins 12 to 20 will be unavailable.

Table 14 Optional Interface Conflicts

		Optional Interfaces																			
		0	1	3	4	5	7	8	9	10	11	12	13	14	15	16	18	19	20	21	
Optional Interfaces	0																				
	1	0																			
	3	+	+																		
	4	+	+	3																	
	5	0	1	+	+																
	7	+	+	+	+	+															
	8	+	+	+	+	+	+														
	9	+	+	+	+	+	7	8													
	10	+	+	+	+	+	+	+	9												
	11	0	1	+	+	+	+	+	+	+											
	12	+	+	+	+	+	+	+	9	10	+										
	13	+	+	+	+	+	7	+	9	10	+	12									
	14	0	1	+	+	+	+	8	9	+	+	+	+								
15	0	1	+	+	5	+	+	+	+	+	+	+	+								
16	+	+	+	+	+	+	+	+	+	+	+	+	+	+							
18	0	1	+	+	5	+	+	+	+	+	+	+	+	15	+						
19	+	+	+	+	+	7	+	9	+	+	+	13	+	+	+	+					
20	+	+	+	+	+	+	8	9	+	+	+	+	+	+	16	+	+				
21	0	1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+			
Def. I/Fs	D1	0	1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	21	
	D2	0	1	3	4	5	7	8	9	10	11	12	13	14	15	16	18	19	20	+	

Key:

+ No conflict. Both functions can operate at the same time.

number The numbered option is enabled. The other option is disabled or the affected default interface is either disabled or restricted.

2.4.5 Optional Interface Pin Arrangements

Tables 15 to 33 on the following pages list the various functions that share pins.

Reading the tables

- ◆ If a pin number is shown next to a pin name then that function/pin is available by default, i.e. with no optional interface function selected by the strap pins during initialisation. The 'Shared with' column indicates which optional interfaces that pin is shared with.
- ◆ If "shared" is shown next to a pin name then that function/signal is only available as an option. The default pin name is shown in the 'Shared with' column. The pin number can be found in [section 2.5, 'Pin Identification', on page 28](#).

Table 15 ROM/GIO Interface

ROM or GIO	Pin name	Pin no.	Description	In/Out	Shared with
ROM and GIO	RADD0	34	Address output	O	0, 1
	RADD1	35		O	
	RADD2	36		O	
	RADD3	37		O	
	RADD4	38		O	
	RADD5	39		O	
	RADD6	40		O	
	RADD7	41		O	
	RADD8	44		O	
	RADD9	45		O	
	RADD10	46		O	
	RADD11	47		O	
	RADD12	48		O	
	RADD13	49		O	
	RADD14	50		O	
	RADD15	51		O	
	RADD16	52		O	
	RADD17	55		O	
	RADD18	56		O	
	RADD19	57		O	0, 1, 21
	RADD20	58		O	
	RADD21	59		O	
	RADD22	60		O	
	RADD23	shared	Extended Address (see also interface option 18, table 32 on page 27)	O	PPORT14
	RADD24	shared		O	PPORT13
	RADD25	shared		O	PPORT12

Table 15 ROM/GIO Interface (Continued)

ROM or GIO	Pin name	Pin no.	Description	In/Out	Shared with
ROM and GIO	RDATA0	15	Data Bus	I/O	0, 1, 21
	RDATA1	16		I/O	
	RDATA2	17		I/O	
	RDATA3	18		I/O	
	RDATA4	19		I/O	
	RDATA5	20		I/O	
	RDATA6	21		I/O	
	RDATA7	22		I/O	
	RDATA8	23		I/O	0, 1
	RDATA9	24		I/O	
	RDATA10	28		I/O	
	RDATA11	29		I/O	
	RDATA12	30		I/O	
	RDATA13	31		I/O	
	RDATA14	32		I/O	
	RDATA15	33		I/O	
	FOEB	61	Output enable for ROM and GIO	O	Not shared
	FWEB	62	Write enable for ROM and GIO	O	
ROM	FCSB0	63	Chip select for ROM	O	Not shared
	<i>FCSB1</i>	<i>shared</i>	<i>Second CS for ROM^A</i>	O	<i>PPORT35</i>
GIO	GCSB0	64	Chip select for GIO	O	Not shared
	<i>GCSB1</i>	<i>shared</i>	<i>Second CS for GIO^A</i>	O	<i>PPORT34</i>
	GRDYB	71	Indicates external device ready	I	0, 1

^A Available only when **Option 12** is enabled.

Table 16 PPORT (Programmable Pin Port)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
(Available by default)	PPORT0	1	General Purpose In/Out port pins	I/O	3, 4
	PPORT1	2		I/O	
	PPORT2	3		I/O	
	PPORT3	4		I/O	
	PPORT4	5		I/O	
	PPORT5	6		I/O	3
	PPORT6	7		I/O	
	PPORT7	8		I/O	
	PPORT8	9		I/O	
	PPORT9	10		I/O	
	PPORT10	13		I/O	
	PPORT11	14		I/O	

Table 16 PPORT (Programmable Pin Port) (Continued)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
(Available by default)	PPORT12	94	General Purpose In/Out port pins (cont.)	I/O	0, 1, 5, 15, 18
	PPORT13	95		I/O	
	PPORT14	96		I/O	
	PPORT15	97		I/O	0, 1, 5, 15
	PPORT16	98		I/O	
	PPORT17	99		I/O	
	PPORT18	100		I/O	0, 1, 5
	PPORT19	101		I/O	
	PPORT20	102		I/O	
	PPORT21	103		I/O	0, 5
	PPORT22	104		I/O	
	PPORT23	105		I/O	0, 1
	PPORT24	106		I/O	0
	PPORT25	107		I/O	0, 1, 11
	PPORT26	108		I/O	
	PPORT27	111		I/O	
	PPORT28	112		I/O	0, 1, 14
	PPORT29	113		I/O	
	PPORT30	118		I/O	8, 9, 14
	PPORT31	119		I/O	
	PPORT32	120		I/O	
	PPORT33	121		I/O	9, 12, 13
	PPORT34	122		I/O	
	PPORT35	123		I/O	9, 10, 12, 13
	PPORT36	124		I/O	13
	PPORT37	125		I/O	
	PPORT38	126		I/O	7, 9, 13
	PPORT39	127		I/O	
	PPORT40	128		I/O	
	PPORT41	129		I/O	7, 9, 13, 19
	PPORT42	130		I/O	7, 9, 19
	PPORT43	131		I/O	8, 9, 20
	PPORT44	132		I/O	16, 20

Table 17 NAND Flash ROM

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Boot option B and Option 21 ^A	NCLE	shared	NAND Command Latch Enable	O	RADD19
	NALE	shared	NAND Address Latch Enable	O	RADD20
	NSEB	shared	NAND Spare area Enable	O	RADD21
	NR/BB	shared	NAND Ready/Busy signal	I	RADD22

Table 17 NAND Flash ROM (Continued)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Boot option B and Option 21	NDATA0	shared	NAND Flash ROM data	I/O	RDATA0
	NDATA1	shared		I/O	RDATA1
	NDATA2	shared		I/O	RDATA2
	NDATA3	shared		I/O	RDATA3
	NDATA4	shared		I/O	RDATA4
	NDATA5	shared		I/O	RDATA5
	NDATA6	shared		I/O	RDATA6
	NDATA7	shared		I/O	RDATA7

A Note that the Write Protect signal (WP) is not supported – this pin on a connected NAND device should be pulled high.

Table 18 PCMCIA

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 0 and Option 1	A0	shared	PCMCIA address	O	RADD0
	A1	shared		O	RADD1
	A2	shared		O	RADD2
	A3	shared		O	RADD3
	A4	shared		O	RADD4
	A5	shared		O	RADD5
	A6	shared		O	RADD6
	A7	shared		O	RADD7
	A8	shared		O	RADD8
	A9	shared		O	RADD9
	A10	shared		O	RADD10
	A11	shared		O	RADD11
	A12	shared		O	RADD12
	A13	shared		O	RADD13
	A14	shared		O	RADD14
	A15	shared		O	RADD15
	A16	shared		O	RADD16
	A17	shared		O	RADD17
	A18	shared		O	RADD18
	A19	shared		O	RADD19
	A20	shared		O	RADD20
	A21	shared		O	RADD21
	A22	shared		O	RADD22
	A23	shared		O	PPORT14
	A24	shared		O	PPORT13
	A25	shared		O	PPORT12

Table 18 PCMCIA (Continued)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 0 and Option 1	D0	shared	PCMCIA data	I/O	RDATA0
	D1	shared		I/O	RDATA1
	D2	shared		I/O	RDATA2
	D3	shared		I/O	RDATA3
	D4	shared		I/O	RDATA4
	D5	shared		I/O	RDATA5
	D6	shared		I/O	RDATA6
	D7	shared		I/O	RDATA7
	D8	shared		I/O	RDATA8
	D9	shared		I/O	RDATA9
	D10	shared		I/O	RDATA10
	D11	shared		I/O	RDATA11
	D12	shared		I/O	RDATA12
	D13	shared		I/O	RDATA13
	D14	shared		I/O	RDATA14
	D15	shared		I/O	RDATA15
	WAITB	shared	Wait signal	I	GRDYB
	CE1B0	shared	Card Enable 1 for slot 0	O	GCSB0
	OEB	shared	Output enable	O	FOEB
	WEB	shared	Write enable	O	FWEB
Option 0	IREQB	shared	Interrupt request	I	PPORT15
	IOIS16B	shared	IO port is 16-bit	I	PPORT16
	CD1B ^A	shared	Card detect for slot 0	I	PPORT17
	CE2B0	shared	Card Enable 2 for slot 0	O	PPORT18
	VS1B ^A	shared	Voltage sense slot 0	I	PPORT19
	IORDB	shared	I/O read	O	PPORT21
	IOWRB	shared	I/O write	O	PPORT22
	RESET ^A	shared	Card reset	O	PPORT23
	INPACKB	shared	Input Port Acknowledge	I	PPORT24
	REGB	shared	Register select and I/O enable	O	PPORT25
	STSCHGB ^A	shared	Card status	I	PPORT29
Option 1	READY	shared	Ready signal	I	PPORT15
	WP	shared	Write Protect	I	PPORT16
	CD1B ^A	shared	Card detect for slot 0	I	PPORT17
	CE2B0	shared	Card Enable 2 for slot 0	O	PPORT18
	VS1B ^A	shared	Voltage sense slot 0	I	PPORT19
	RESET ^A	shared	Card reset	O	PPORT23
	REGB	shared	Register select	O	PPORT25
	BVD1 ^A	shared	Battery Voltage Detect slot 0	I	PPORT29

A Note that pins CD1B, VS1B, RESET, STSCHGB, and BVD1 are controlled by the GPIO port.

Table 19 Parallel TS Interface

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 3	STPCLK	shared	Bit stream input clock	I	PPORT0
	STPEN	shared	Bit-stream input enable	I	PPORT1
	STPERRB	shared	TS error input	I	PPORT2
	STPSTRT	shared	TS sync start	I	PPORT3
	STPDAT0	shared	TS bit-stream input data	I	PPORT4
	STPDAT1	shared		I	PPORT5
	STPDAT2	shared		I	PPORT6
	STPDAT3	shared		I	PPORT7
	STPDAT4	shared		I	PPORT8
	STPDAT5	shared		I	PPORT9
	STPDAT6	shared		I	PPORT10
	STPDAT7	shared		I	PPORT11

Table 20 Serial TS Interface

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 4	STSClk	shared	Bit stream input clock	I	PPORT0
	STSEN	shared	Bit-stream input enable	I	PPORT1
	STSERRB	shared	TS error input	I	PPORT2
	STSSTRT	shared	TS sync start	I	PPORT3
	STSDAT	shared	TS data	I	PPORT4

Table 21 High Speed Data (HSD) output port

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 5	HSD0	shared	High Speed Data output port	O	PPORT19
	HSD1	shared		O	PPORT18
	HSD2	shared		O	PPORT17
	HSD3	shared		O	PPORT16
	HSD4	shared		O	PPORT15
	HSD5	shared		O	PPORT14
	HSD6	shared		O	PPORT13
	HSD7	shared		O	PPORT12
	HSDCLK	shared	High Speed Data clock	O	PPORT22
	HSDE	shared	High Speed Data output enable	O	PPORT21
	PKTSTRT	shared	Indicates TS sync byte output	O	PPORT20

Table 22 Smart Card 0

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 7	SMRST0	shared	Card reset	O	PPORT38
	CMDVCC0	shared	VCC control	O	PPORT39
	OFF0	shared	Card detect	I	PPORT40
	SMCLK0	shared	Data clock	I/O	PPORT41
	SMDAT0	shared	Data	I/O	PPORT42

Table 23 Smart Card 1

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 8	SMRST1	shared	Card reset	O	PPORT30
	CMDVCC1	shared	VCC control	O	PPORT31
	OFF1	shared	Card detect	I	PPORT32
	SMCLK1	shared	Data clock	I/O	PPORT33
	SMDAT1	shared	Data	I/O	PPORT43

Table 24 Digital Video Output

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 9	VCK	shared	Internal video pixel clock	O	PPORT40
	VD00	shared	Digital video Y/Cb/Cr data	O	PPORT30
	VD01	shared		O	PPORT31
	VD02	shared		O	PPORT32
	VD03	shared		O	PPORT33
	VD04	shared		O	PPORT34
	VD05	shared		O	PPORT35
	VD06	shared		O	PPORT38
	VD07	shared		O	PPORT39
	CSYNC/ VVS	shared	Composite sync for RGB SCART/ Internal vertical sync signal	O	PPORT41
	BLANK/ VHS	shared	Blanking signal for RGB SCART/ Internal horizontal sync signal	O	PPORT42
	VFIELD	shared	Field index signal for RGB SCART	O	PPORT43

Table 25 Timer

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 10	CAP/COMP0	shared	Capture timer input / Compare timer output	I/O	PPORT35

Table 26 Clocked Serial Interface (CSI)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 11	SDIN	shared	Serial data input	I	PPORT25
	SDOUT	shared	Serial data output	O	PPORT26
	SCKINOUT	shared	Serial clock input/output	I/O	PPORT27

Table 27 Additional ROM/GIO Chip Select^A

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 12	GC5B1	shared	Additional GIO Chip Select	O	PPORT34
	FCSB1	shared	Additional ROM Chip Select	O	PPORT35

A See also [table 15 on page 19](#).

Table 28 Fast UART 0

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 13	RTS0B	shared	Request to send	O	PPORT34
	CTS0B	shared	Clear to send	I	PPORT35
	RXD0B	shared	Receive data	I	PPORT36
	TXD0B	shared	Transmit data	O	PPORT37
	RI0B	shared	Ring indicator	I	PPORT38
	DCD0B	shared	Data carrier detect	I	PPORT39
	DTR0B	shared	Data terminal ready	O	PPORT40
	DSR0B	shared	Data set ready	I	PPORT41

Table 29 Fast UART 1a (Standard pinning)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 14	RTS1B	shared	Request to send	O	PPORT28
	CTS1B	shared	Clear to send	I	PPORT29
	RI1B	shared	Ring indicator	I	PPORT30
	DCD1B	shared	Data carrier detect	I	PPORT31
	DTR1B	shared	Data terminal ready	O	PPORT32
	DSR1B	shared	Data set ready	I	PPORT33
	RXD1B	147	Receive data	I	Not shared
	TXD1B	148	Transmit data	O	

The RXD1B and TXD1B pins in the UART1 interface are not shared and so the UART1 i/f is also listed in [table 13 on page 17](#).

Table 30 Fast UART 1b (Alternate pinning)

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 15	RTS1B	shared	Request to send	O	PPORT12
	CTS1B	shared	Clear to send	I	PPORT13
	RI1B	shared	Ring indicator	I	PPORT14
	DCD1B	shared	Data carrier detect	I	PPORT15
	DTR1B	shared	Data terminal ready	O	PPORT16
	DSR1B	shared	Data set ready	I	PPORT17
	RXD1B	147	Receive data	I	Not shared
	TXD1B	148	Transmit data	O	

Table 31 Infrared Interface

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 16	IR_IN0	shared	Infrared receiver input	I	PPORT44

Table 32 Extended ROM/GIO Addressing^A

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 18	RADD25	shared	Additional ROM/GIO address pins	O	PPORT12
	RADD24	shared		O	PPORT13
	RADD23	shared		O	PPORT14

A See also [table 15 on page 19](#).

Table 33 External Data Latch

I/F Option	Pin name	Pin no.	Description	In/Out	Shared with
Option 19	EX_CLK0	shared	External latch clock	O	PPORT41
	EX_OE0	shared	External latch output enable	O	PPORT42
Option 20	EX_CLK1	shared	External latch clock	O	PPORT43
	EX_OE1	shared	External latch output enable	O	PPORT44

2.5 Pin Identification

The following table lists all the device pins by pin number. Pins are named by their default function.

Table 34 Global Pin List

No	Name	Type	No	Name	Type	No	Name	Type
1	PPORT0	2	40	RADD6	1	79	VACVBS	D
2	PPORT1	2	41	RADD7	1	80	DAVDD01	VAD
3	PPORT2	2	42	GND1	G	81	RSET0	DR
4	PPORT3	2	43	VDD1	V1	82	REF0	DS
5	PPORT4	2	44	RADD8	1	83	DAGND1	GAD
6	PPORT5	2	45	RADD9	1	84	REF1	DS
7	PPORT6	2	46	RADD10	1	85	RSET1	DR
8	PPORT7	2	47	RADD11	1	86	DAVDD11	VAD
9	PPORT8	2	48	RADD12	1	87	VAPR	D
10	PPORT9	2	49	RADD13	1	88	DAGND12	GAD
11	GND1	G	50	RADD14	1	89	DAVDD12	VAD
12	VDD1	V1	51	RADD15	1	90	VAPB	D
13	PPORT10	2	52	RADD16	1	91	DAGND13	VAD
14	PPORT11	2	53	VDD3	V3	92	GND3	G
15	RDATA0	1	54	GND3	G	93	VDD3	V3
16	RDATA1	1	55	RADD17	1	94	PPORT12	2
17	RDATA2	1	56	RADD18	1	95	PPORT13	2
18	RDATA3	1	57	RADD19	1	96	PPORT14	2
19	RDATA4	1	58	RADD20	1	97	PPORT15	2
20	RDATA5	1	59	RADD21	1	98	PPORT16	2
21	RDATA6	1	60	RADD22	1	99	PPORT17	2
22	RDATA7	1	61	FOEB	9	100	PPORT18	2
23	RDATA8	1	62	FWEB	9	101	PPORT19	2
24	RDATA9	1	63	FCSB0	9	102	PPORT20	2
25	VDD3	V3	64	GCSB0	9	103	PPORT21	2
26	GND3	G	65	AMCK	8	104	PPORT22	2
27	VDD3	V3	66	VDD1	V1	105	PPORT23	2
28	RDATA10	1	67	ABCK	8	106	PPORT24	2
29	RDATA11	1	68	ATX	1	107	PPORT25	2
30	RDATA12	1	69	ADO	8	108	PPORT26	2
31	RDATA13	1	70	ALRCK	8	109	VDD3	V3
32	RDATA14	1	71	GRDYB	4	110	GND3	G
33	RDATA15	1	72	TEST	5	111	PPORT27	2
34	RADD0	1	73	VDD1	V1	112	PPORT28	2
35	RADD1	1	74	GND1	G	113	PPORT29	2
36	RADD2	1	75	DAGND03	GAD	114	SDA0	10
37	RADD3	1	76	VAY	D	115	SCL0	10
38	RADD4	1	77	DAVDD02	VAD	116	SDA1	10
39	RADD5	1	78	DAGND02	GAD	117	SCL1	10

No	Name	Type	No	Name	Type	No	Name	Type
118	PPORT30	2	151	JTMS	4	184	GND2	G
119	PPORT31	2	152	JTCK	4	185	VDD2	V2
120	PPORT32	2	153	JTRST	4	186	DADD3	3
121	PPORT33	2	154	GND2	G	187	DADD2	3
122	PPORT34	2	155	VDD2	V2	188	DADD1	3
123	PPORT35	2	156	DQ15	3	189	DADD0	3
124	PPORT36	2	157	DQ14	3	190	DADD10	3
125	PPORT37	2	158	DQ13	3	191	DBA1	3
126	PPORT38	2	159	DQ12	3	192	DBA0	3
127	PPORT39	2	160	DQ11	3	193	GND2	G
128	PPORT40	2	161	DQ10	3	194	VDD2	V2
129	PPORT41	2	162	GND2	G	195	DCSB	3
130	PPORT42	2	163	GND2	G	196	DRASB	3
131	PPORT43	2	164	VDD2	V2	197	DCASB	3
132	PPORT44	2	165	DQ9	3	198	DWEB	3
133	VDD1	V1	166	DQ8	3	199	DQM0	3
134	PAGND	GAP	167	DQS1	3	200	DADD13	3
135	PAVDD	VAP	168	N/C		201	N/C	
136	XT2	OSC	169	DQM1	3	202	DQ7	3
137	XT1	OSC	170	N/C		203	DQ6	3
138	PAGND	GAP	171	DCLK	3	204	DQ5	3
139	PAVDD	VAP	172	DCKE	3	205	VDD2	V2
140	CLK27IN	4	173	DADD12	3	206	GND2	G
141	GND1	G	174	DADD11	3	207	VDD1	V1
142	VDD3	V3	175	VDD2	V2	208	DQ4	3
143	PWMOUT	7	176	GND2	G	209	DQ3	3
144	RSTOUT	8	177	VDD1	V1	210	DQ2	3
145	RSTSWB	5	178	DADD9	3	211	DQ1	3
146	NMI	5	179	DADD8	3	212	DQ0	3
147	RXD1B	4	180	DADD7	3	213	VDD2	V2
148	TXD1B	8	181	DADD6	3	214	GND2	G
149	JTDI	4	182	DADD5	3	215	GND3	G
150	JTDO	9	183	DADD4	3	216	VDD3	V3

Table 35 Key to pin types

Code	Description
1	9mA normal bi-directional buffer
2	9mA Schmitt input bi-directional buffer
3	Bi-directional LVTTL buffer (TDZE247)
4	Normal input buffer
5	Schmitt input buffer
7	6mA output buffer
8	9mA output buffer
9	9mA tri-state output buffer
10	9mA bi-directional N-channel open-drain I ² C buffer
D	Analog Video output
DS	Analog video: external voltage reference
DR	Analog video: resistor for adjusting full scale currents
G	GND = Main supply ground
GAD	DAGNDx = Analog ground for video DAC
GAP	PAGND = Ground for PLL
OSC	Oscillator with EN (3.3V, 16~32MHz)
V1	V _{DD1} = 1.5V (core)
V2	V _{DD2} = 3.3V for Unified Memory I/F buffers
V3	V _{DD3} = 3.3V for IO buffers
VAP	PAV _{DD} = V _{DD} (1.5V) for PLL
VAD	AV _{DD} = Analog V _{DD} (3.3V) for video DACs

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

For each parameter, this defines the limit value that must not be exceeded even for a moment. If a parameter is exceeded even for a moment, the device may be degraded or destroyed. Please ensure that the absolute maximum ratings are never exceeded.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Supply Voltage Core	V _{DD1}	1.5V	-0.5	—	2.0	V	
Supply Voltage I/O buffers	V _{DD2}	3.3V	-0.5	—	4.6	V	
Supply Voltage PLL	PAV _{DD}	1.5V	-0.5	—	2.0	V	
Supply Voltage Video DAC	VAV _{DD}	3.3V	-0.5	—	4.6	V	
Input Voltage1	V _{in}	3.3V Input Buffer	-0.5	—	4.6	V	V _{in} < V _{DD2} + 0.5V
Output Voltage2	V _{out}	3.3V Buffer	-0.5	—	4.6	V	V _{out} < V _{DD2} + 0.5V
Storage Temperature	T _{stg}		-55	—	+125	°C	

3.2 Recommended Operating Range

For each parameter, this defines the range within which the device will operate normally. Operation with any parameter outside these ranges may lead to instability or reduced reliability.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Supply Voltage: Video DACs	VAV _{DD}	3.3V	3.14	3.3	3.46	V	
Supply Voltage: Core	V _{DD1}	1.5V	1.43	1.5	1.57	V	
Supply Voltage: I/O buffers	V _{DD2}	3.3V	3.14	3.3	3.46	V	
Ambient Operating Temp.	T _a		0	—	70	°C	

3.2.1 Power-on sequence

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Delay time: V _{DD2} to V _{DD1}	n/a	-100	—	100	ms	

3.3 DC Characteristics – General

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Input-High Voltage	V _{IH}	Schmitt trigger input RSTSWB, PPORT[0:44]	2.4	—	V _{DD2}	V	
Input-Low Voltage	V _{IL}	Schmitt trigger input RSTSWB, PPORT[0:44]	0	—	0.6	V	
High Level Output Voltage	V _{OH}	3.3V I/F pins	2.4	—	—	V	I _{OH} = -3mA
Low Level Output Voltage	V _{OL}	3.3V I/F pins	—	—	0.4	V	I _{OL} = 9mA
Input Leakage Current	I _{HI}	V _I = V _{DD2}	-10	—	+10	μA	
Input Leakage Current	I _{LI}	V _I = GND	-10	—	+10	μA	

3.4 DC Characteristics – Unified Memory Interface

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Input High Level Voltage	V _{IH}		2.4	–	V _{DD2}	V	
Input Low Level Voltage	V _{IL}		0	–	0.6	V	
High Level Output Voltage	V _{OH}		2.4	–	–	V	I _{OH} = -3mA
Low Level Output Voltage	V _{OL}		–	–	0.4	V	I _{OL} = 9mA

3.5 DC Characteristics – I²C Interface

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units	Notes
Input High Level Voltage	V _{IH}	Standard	0.7 x V _{DD2}	–	V _{DD2} +0.5	V	
		Fast	0.7 x V _{DD2}	–	V _{DD2} +0.5	V	
Input Low Level Voltage	V _{IL}	Standard	–0.5	–	0.3 x V _{DD2}	V	
		Fast	–0.5	–	0.3 x V _{DD2}	V	
Hysteresis of Schmitt trigger inputs	V _{HYS}	Standard	n/a	n/a	n/a	V	
		Fast	0.05 x V _{DD2}	–	–	V	
Low Level output voltage (Open Drain)	V _{OL}	Standard	0	–	0.4	V	9mA sink current
		Fast	0	–	0.4	V	

3.6 DAC Characteristics – Analog Video Outputs

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Output load	R _{LOAD}		–	200	–	Ω	
Supply Current	I _{DDA}		–	40	–	mA	4 channels total
Resolution	N		–	10	–	Bits	
Integral Non Linearity	ILE		–2.0	–	+2.0	LSB	
Differential Non Linearity	DLE		–2.0	–	+2.0	LSB	
Full-scale current	F _{SC}	V _{REF} = 1.32V, R _{SET} = 910Ω, R _{LOAD} = 200Ω	6.4	6.6	6.8	mA	
Full-scale voltage	F _{SV}		1.28	1.32	1.36	V	

Full-scale voltage

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

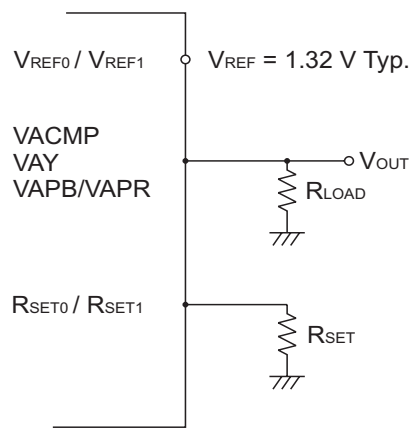
$$R_{LOAD} = 200\Omega$$

$$I_{OUT} = (V_{REF} \times K) / R_{SET}$$

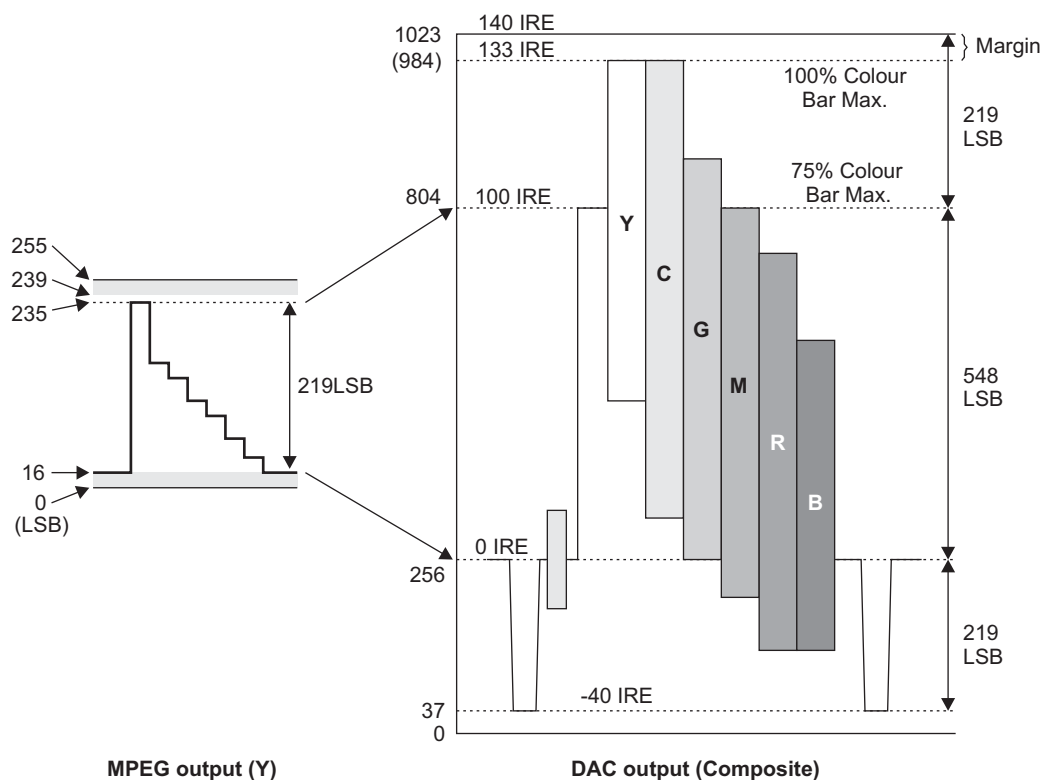
$$K = 4.55$$

$$V_{REF} = 1.32V \text{ Typ.}$$

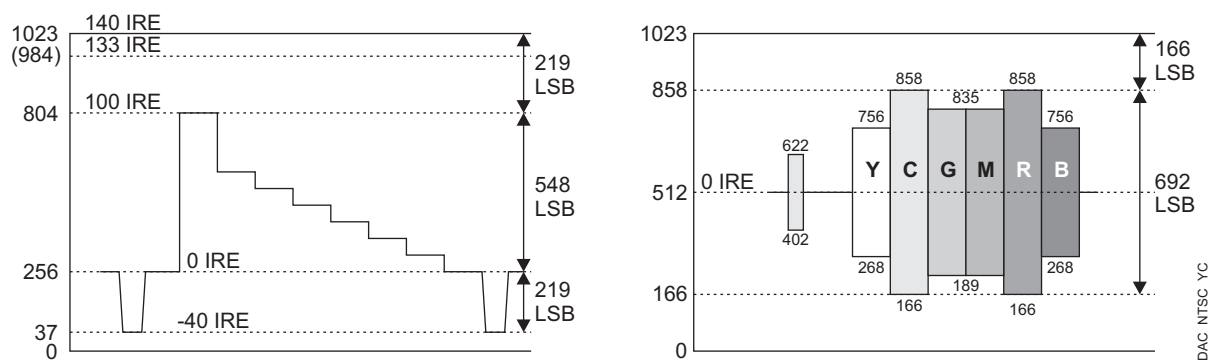
$$R_{SET} = 910\Omega$$



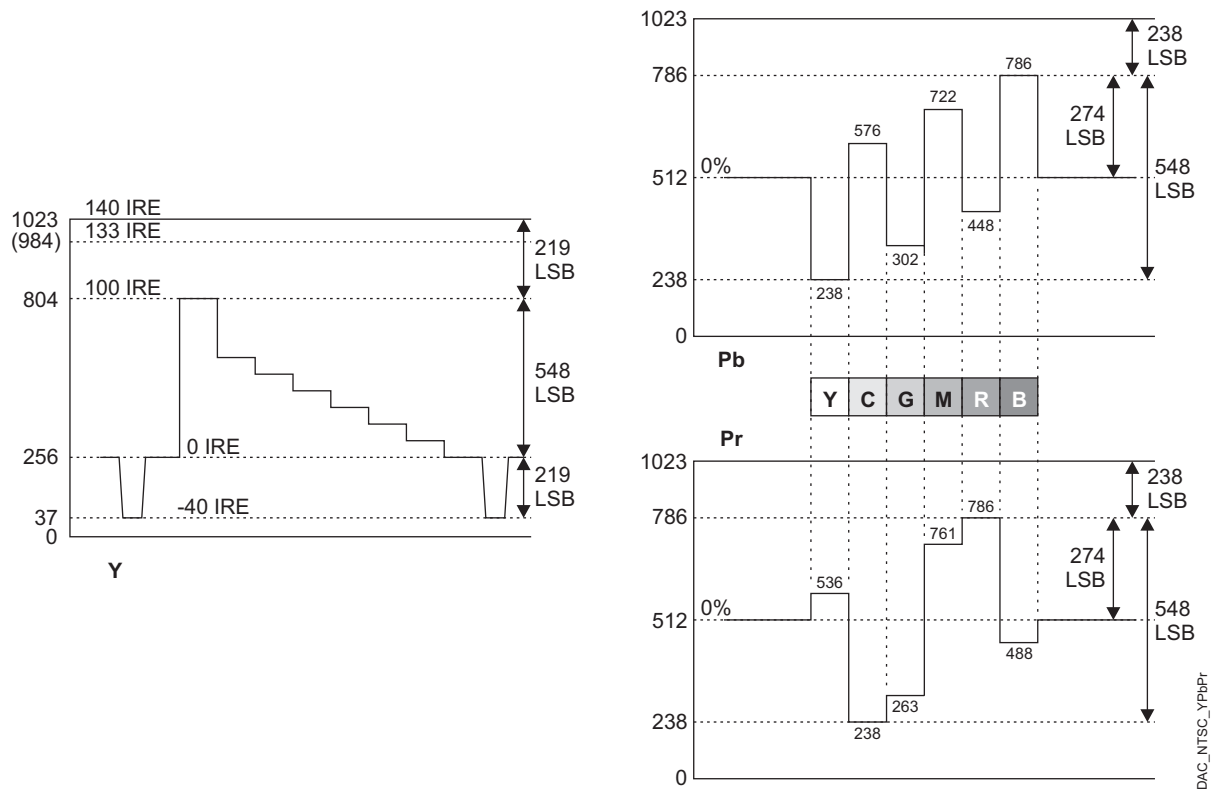
3.6.1 NTSC – Composite output



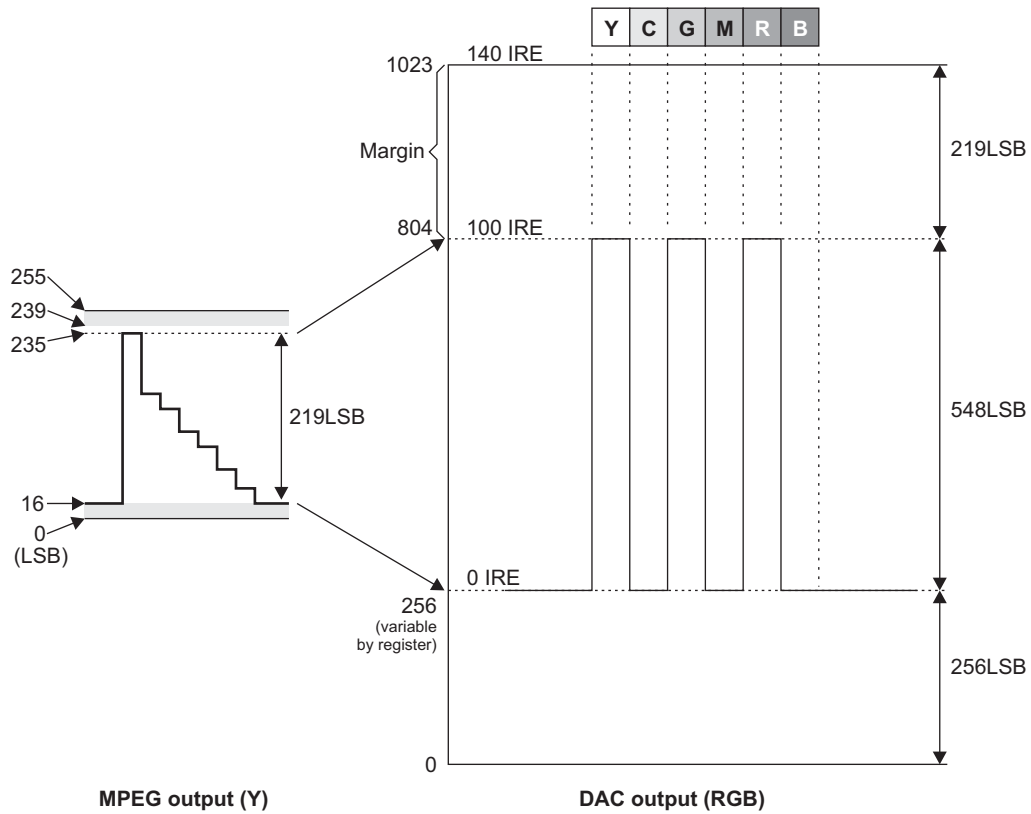
3.6.2 NTSC – Y/C output



3.6.3 NTSC – Y/Pb/Pr output

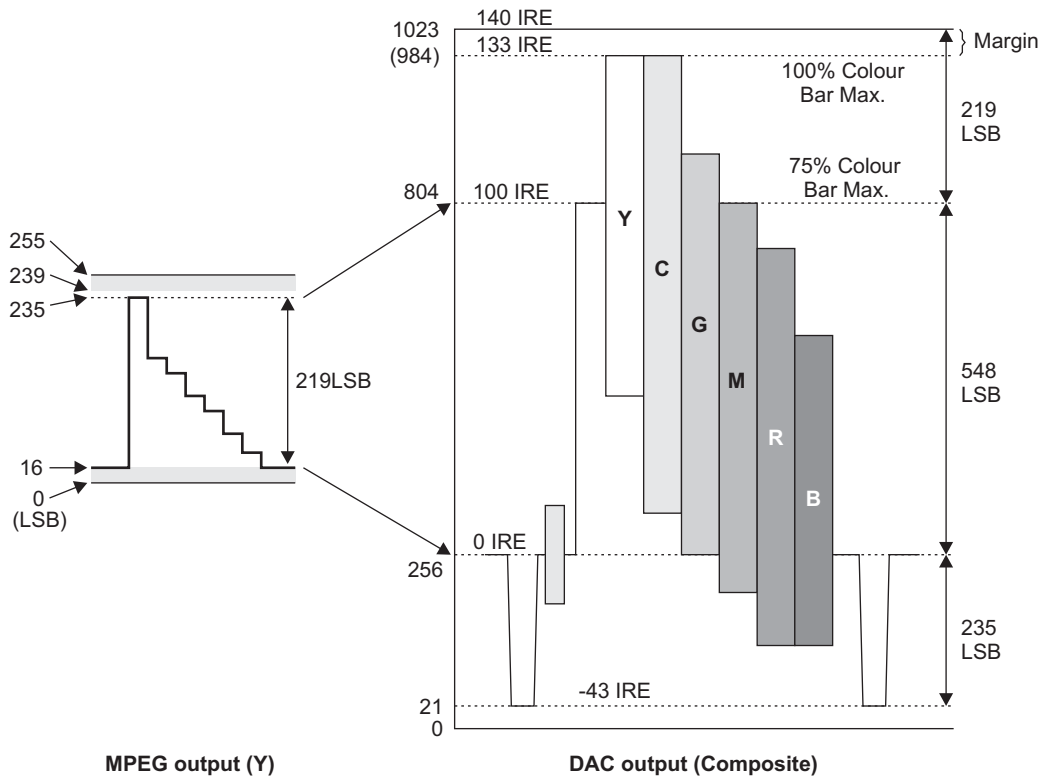


3.6.4 NTSC – RGB output



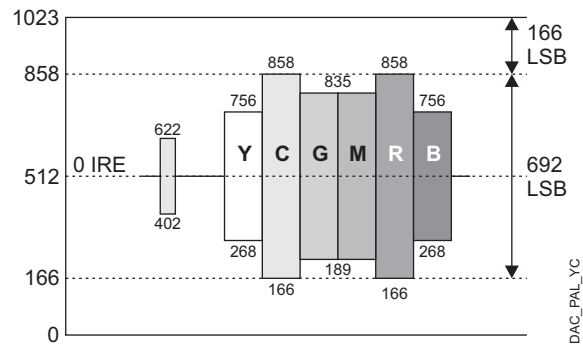
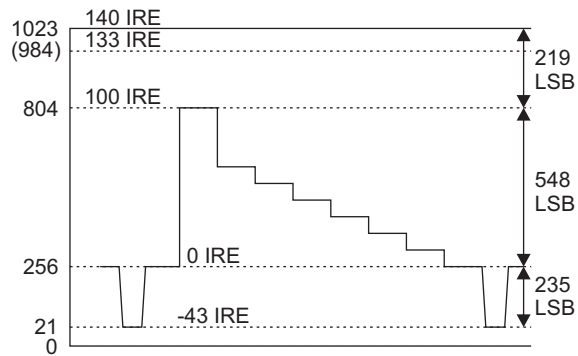
DAC_NTSC_RGB

3.6.5 PAL – Composite output

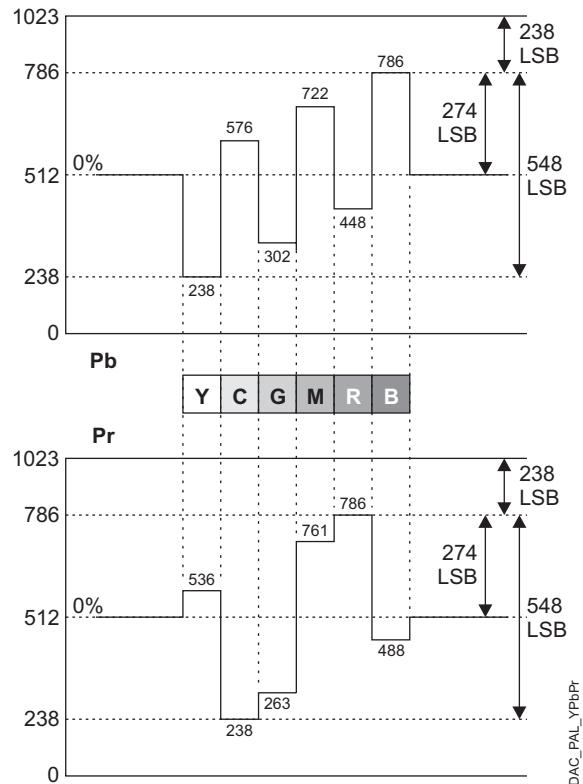
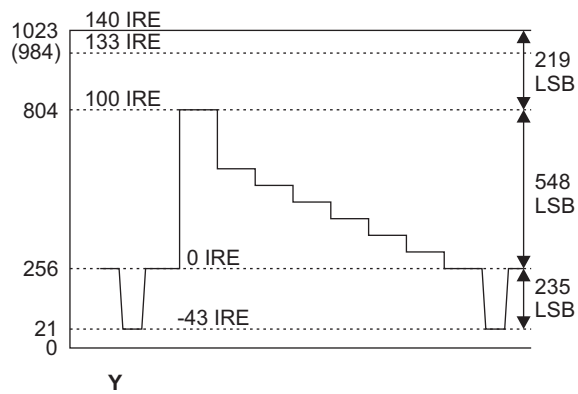


DAC_PAL_COMP

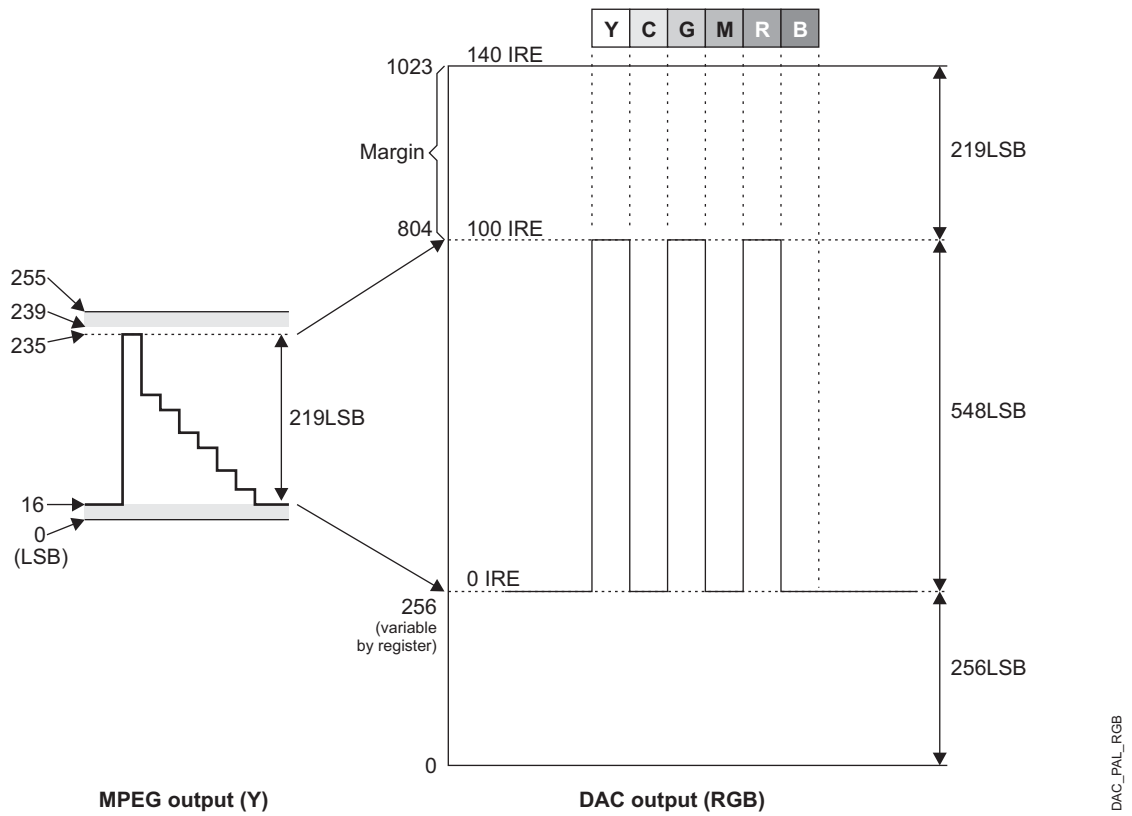
3.6.6 PAL – Y/C output



3.6.7 PAL – Y/Pb/Pr output



3.6.8 PAL – RGB output

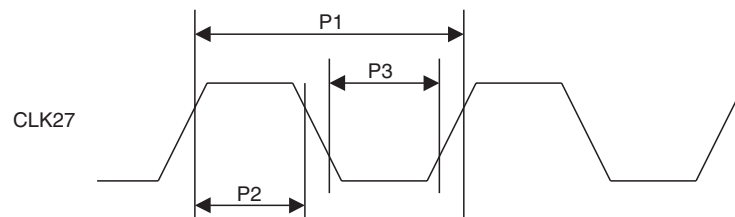


4 AC TIMING SPECIFICATIONS

4.1 System

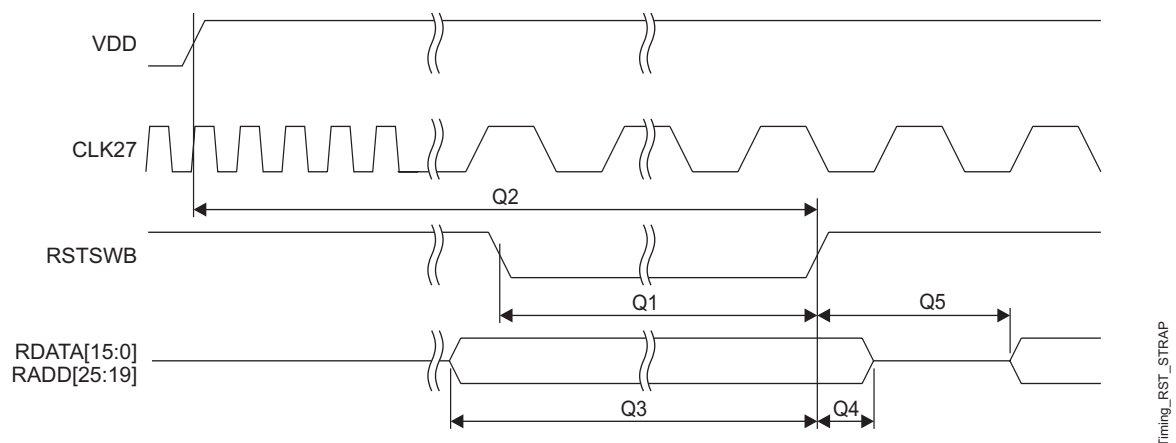
4.1.1 27MHz Clock

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Clock frequency	P1	–	27	–	MHz	
CLK27 high level width	P2	16.6	–	–	ns	
CLK27 low level width	P3	16.6	–	–	ns	



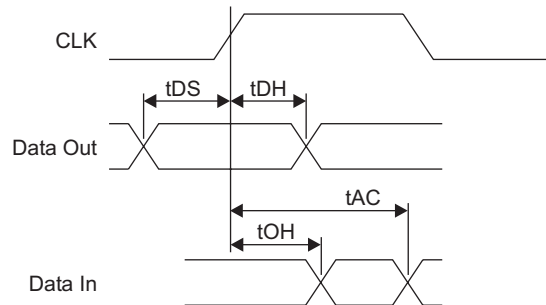
4.1.2 Reset and Strap Input Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
RSTSWB low level width	Q1	10	–	–	ms	
RSTSWB high inactive time	Q2	100	–	–	ms	
Strap data set-up time	Q3	500	–	–	μs	
Strap data hold time	Q4	200	–	–	ns	
Data output start	Q5	1	–	–	μs	



4.2 Unified Memory Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Clock cycle time	tCK	7.0	–	–	ns	
Access time from CLK	tAC	–	–	tCK - 0.50	ns	
Data In hold time	tOH	2.5	–	–	ns	
Data Out setup time	tDS	2.0	–	–	ns	
Data Out hold time	tDH	1.5	–	–	ns	



Timing_SDRAM

4.3 ROM Interface

4.3.1 NOR Flash ROM

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Address setup to FCSB	F1	1.5*(2T)	–	–	ns	
FCSB to FOEB delay for Active Level	F2	0.5*(2T)	–	–	ns	
FCSB to FWEB delay for Active Level	F3	0.5*(2T)	–	–	ns	
FOEB Active time	F4	N*(2T)	–	–	ns	
FWEB Active time	F5	N*(2T)	–	–	ns	
Address hold to FCSB	F6	0.5*(2T)	–	–	ns	
FCSB High time	F7	2*(2T)	–	–	ns	
FOEB to FCSB delay for Inactive Level	F8	0	–	–	ns	
FWEB to FCSB delay for Inactive Level	F9	0	–	–	ns	
Read Data Hold Time	F10	0.5*(2T)	–	–	ns	
Write Data Hold Time	F11	2*(2T)	–	–	ns	
Read Data Setup Time	F12	2T	–	–	ns	
Write Data Setup Time	F13	2T	–	–	ns	

Where:

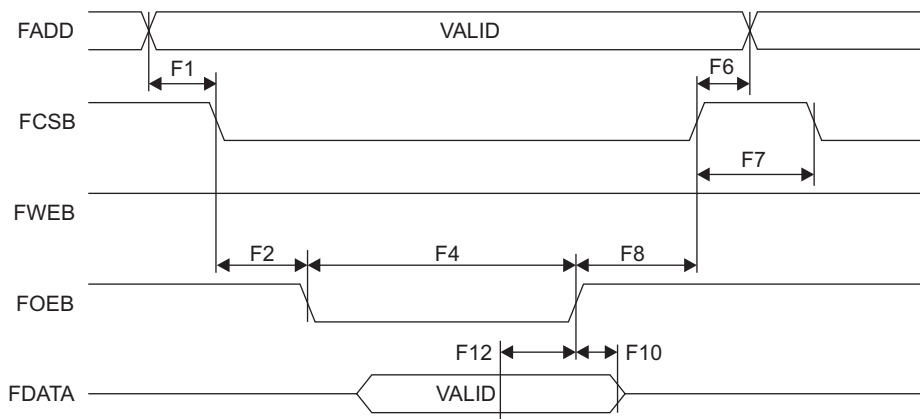
N = FAT (programmable as 2, 3, 4, 6, 8, 10, 12, 14, 16 or 18)

T = VRCLK period (5.35ns @ 187MHz, 6.02ns @ 166MHz)

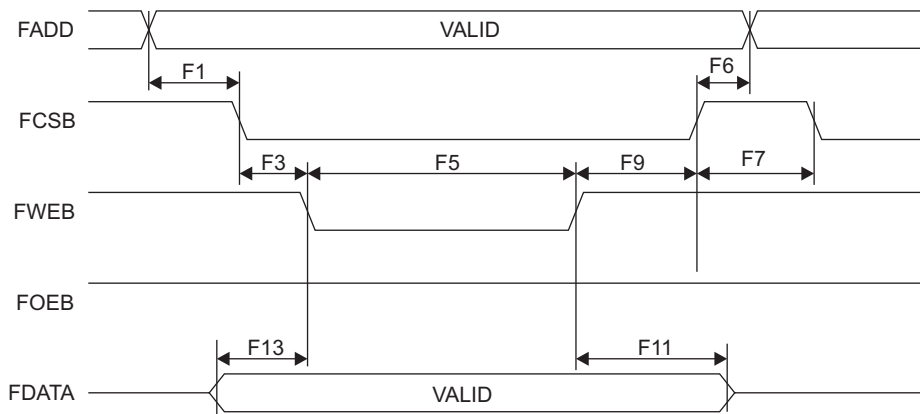
For the recommended settings of FAT = 8 and VRCLK = 187MHz:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Address setup to FCSB	F1	15	–	–	ns	
FCSB to FOEB delay for Active Level	F2	5	–	–	ns	
FCSB to FWEB delay for Active Level	F3	5	–	–	ns	
FOEB Active time	F4	85	–	–	ns	
FWEB Active time	F5	85	–	–	ns	
Address hold to FCSB	F6	5	–	–	ns	
FCSB High time	F7	21	–	–	ns	
FOEB to FCSB delay for Unactive Level	F8	0	–	–	ns	
FWEB to FCSB delay for Unactive Level	F9	0	–	–	ns	
Read Data Hold Time	F10	5	–	–	ns	
Write Data Hold Time	F11	20	–	–	ns	
Read Data Setup Time	F12	10	–	–	ns	
Write Data Setup Time	F13	10	–	–	ns	

Read Timing – NOR Flash ROM



Write Timing – NOR Flash ROM



4.3.2 NAND Flash ROM

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
CLE to FWEB for Active Level	F1	2T	–	–	ns	
CLE to FWEB for Unactive Level	F2	3*(2T)	–	–	ns	
FCSB to FWEB for Active Level (Command Latch Cycle)	F3	1.5*(2T)	–	–	ns	
FCSB to FWEB for Unactive Level	F4	4.5*(2T)	–	–	ns	
FWEB Active Time	F5	N*(2T)	–	–	ns	
Write Data Setup Time for Command Latch Cycle	F6	N*(2T)	–	–	ns	
Write Data Hold Time for Command Latch Cycle	F7	3*(2T)	–	–	ns	
FCSB to FWEB for Active Level (Address Latch Cycle)	F8	0.5*(2T)	–	–	ns	
FWEB Access Time	F9	(N+3)*(2T)	–	–	ns	
FEW to ALE for Unactive Level (Address Latch Cycle)	F10	2*(2T)	–	–	ns	
FEW to ALE for Active Level (Address Latch Cycle)	F11	2T	–	–	ns	
Write Data Setup Time for Address Latch Cycle	F12	(N+1)*(2T)	–	–	ns	
Write Data Hold Time for Address Latch Cycle	F13	2*(2T)	–	–	ns	
FOEB Access Time	F14	(N+1)*(2T)	–	–	ns	
Read Data Setup Time for Read Cycle	F15	2T	–	–	ns	
Read Data Hold Time for Read Cycle	F16	0.5*(2T)	–	–	ns	
FWEB Access Time for Write Operation	F17	(N+1)*(2T)	–	–	ns	
CLE to FWEB delay for Page Program Command	F18	2T	–	–	ns	
FWEB to FCSB delay for Release CS	F19	4.5*(2T)	–	–	ns	

Where:

N = FAT (programmable as 2, 3, 4, 6, 8, 10, 12, 14, 16 or 18)

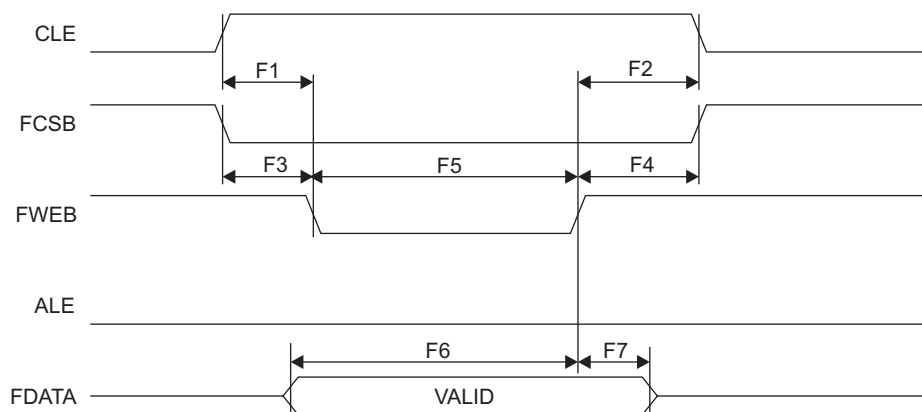
T = VRCLK period (5.35ns @ 187MHz, 6.02ns @ 166MHz)

For the recommended settings of FAT = 6 and VRCLK = 187MHz:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
CLE to FWEB for Active Level	F1	10	–	–	ns	
CLE to FWEB for Unactive Level	F2	30	–	–	ns	
FCSB to FWEB for Active Level (Command Latch Cycle)	F3	15	–	–	ns	
FCSB to FWEB for Unactive Level	F4	45	–	–	ns	
FWEB Active Time	F5	60	–	–	ns	
Write Data Setup Time for Command Latch Cycle	F6	60	–	–	ns	
Write Data Hold Time for Command Latch Cycle	F7	30	–	–	ns	

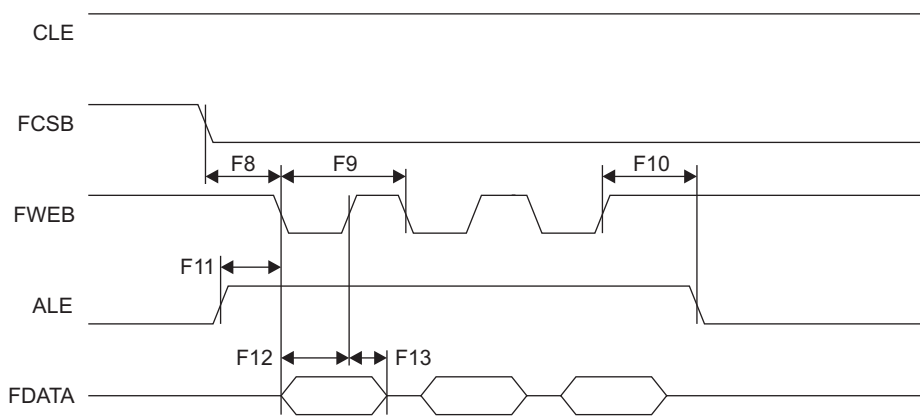
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
FCSB to FWEB for Active Level (Address Latch Cycle)	F8	5	–	–	ns	
FWEB Access Time	F9	60	–	–	ns	
FEW to ALE for Unactive Level (Address Latch Cycle)	F10	20	–	–	ns	
FEW to ALE for Active Level (Address Latch Cycle)	F11	10	–	–	ns	
Write Data Setup Time for Address Latch Cycle	F12	70	–	–	ns	
Write Data Hold Time for Address Latch Cycle	F13	20	–	–	ns	
FOEB Access Time	F14	85	–	–	ns	
Read Data Setup Time for Read Cycle	F15	10	–	–	ns	
Read Data Hold Time for Read Cycle	F16	15	–	–	ns	
FWEB Access Time for Write Operation	F17	85	–	–	ns	
CLE to FWEB delay for Page Program Command	F18	10	–	–	ns	
FWEB to FCSB delay for Release CS	F19	45	–	–	ns	

Command Latch Cycle Time for NAND Flash ROM



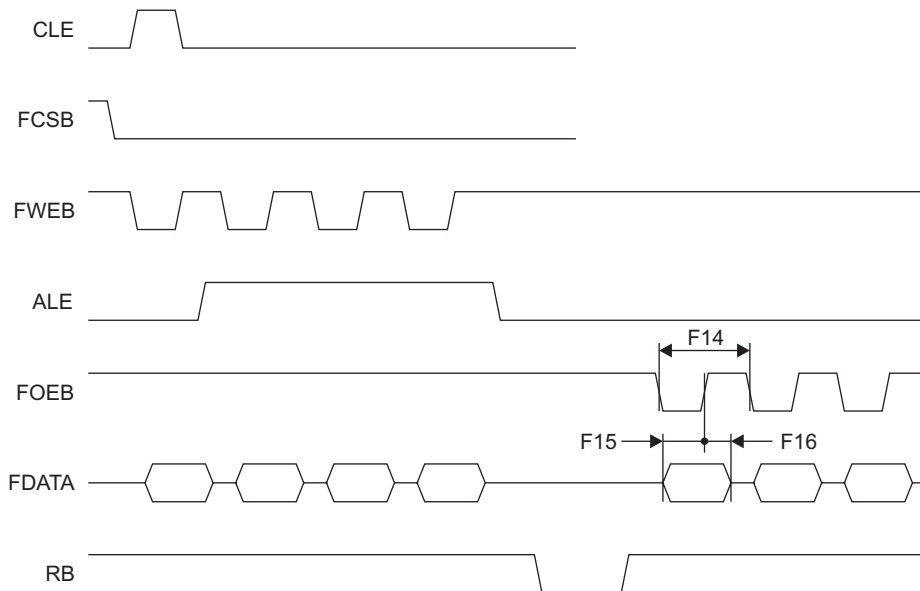
Timing_CMD_Latch_NAND

Address Latch Cycle Time for NAND Flash ROM



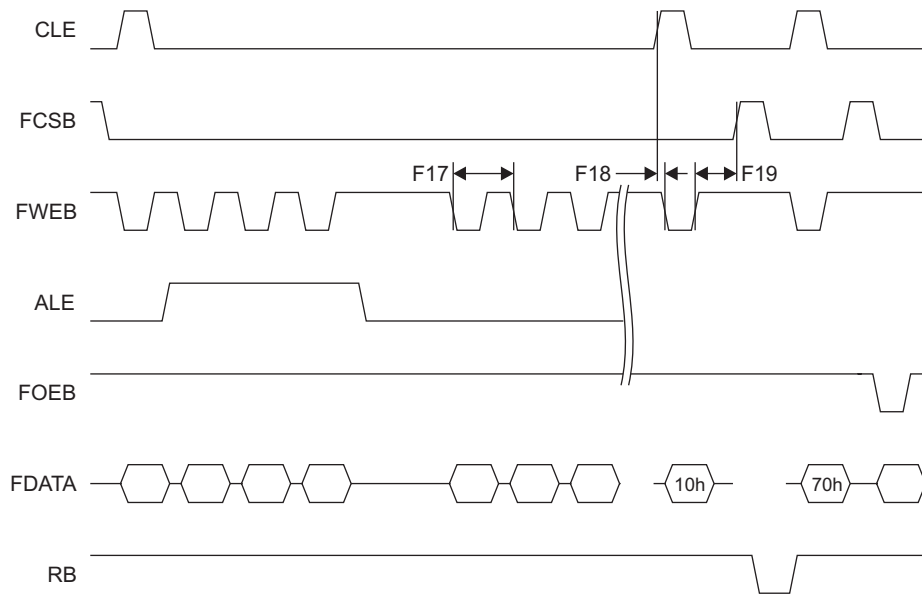
Timing_ADDR_Latch_NAND

Read Operation for NAND Flash ROM



Timing_NAND_read

Write Operation for NAND Flash ROM



Timing_NAND_write

4.4 General IO Interface

4.4.1 Motorola and Intel Modes

Parameter	Symbol	Min	Typ	Max	Unit
Address set-up time prior to GCSB	G1	$N*2T - T (-Dcs_down*2T)$	—	—	ns
Address set-up time prior to GOEB	G2	$N*2T - T (-Dcs_down*2T + Doe_down*2T)$	—	—	ns
Address set-up time prior to GWEB	G3	$N*2T - T (-Dcs_down*2T + Dwe_down*2T)$	—	—	ns
GOEB width	G4	$(AW + 1)*2T - T (-Doe_down*2T + Doe_up*2T)$	—	—	ns
GWEB width	G5	$(AW + 1)*2T - T (-Dwe_down*2T + Dwe_up*2T)$	—	—	ns
Address hold time prior to GCSB	G6	$N*2T - T (-Dcs_up*2T)$	—	—	ns
GCSB high level width	G7	$N*6T - T (-Dcs_up*2T + Dcs_down*2T)$	—	—	ns
Address hold time after GOEB	G8	$N*2T - T (-Doe_up*2T + Dcs_up*2T - 2T)$	—	—	ns
Address hold time after GWEB	G9	$N*2T - T (-Dwe_up*2T + Dcs_up*2T)$	—	—	ns
Read Data hold time to GOEB	G10	0	—	—	ns
Write Data hold time to GWEB	G11	$N*4T - T (-Dwe_up*2T)$	—	—	ns
Read Data Setup time to GOEB	G12	4T	—	—	ns
Write Data Setup time to GWEB	G13	$N*4T - T (+Dwe_down*2T)$	—	—	ns
Delay time FOEB/FWEB after GRDYB	G14	$N*2T$	—	—	ns
GRDY/WAIT width	G15	$N*2T$	—	—	ns
Wait width	G15A	—	—	$(AW + 1)*2T - T$	ns
FOEB/FWEB no-active assert time after GRDYB no-active	G15B	$N*2T$	—	—	ns
GRDYB non-active width	G15C	0	—	$N*8T$	ns
GRDYB active width	G15D	0	—	—	ns
GCSB to GWEB negative assert time at Motorola write mode	G16	0	—	—	ns
GCSB to GWEB positive assert time	G17	0	—	—	ns

Where:

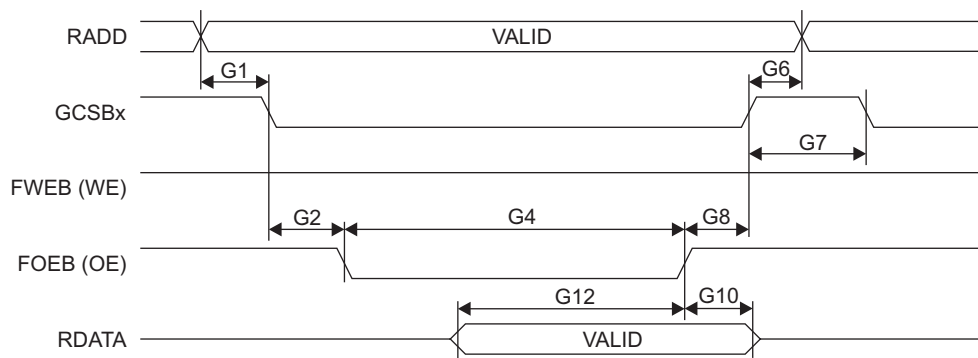
T = VRCLK period (5.34ns @ 187.3125MHz or 6.01ns @ 166.5MHz)
 N = GAT value in RCLK periods (programmable as 32, 2, 3, 4, 8, 16, 24 or 64)
 AW = ACTIVE_WAIT = 32, 2, 3, 4, 8, 16, 24 or 64 RCLKs
 Dcs_up/Dcs_down = CS0~4DELAY = 0, 1, 2 or 3 (recommended setting: 0)
 Doe_up/Doe_down = OEBDELAY = 0, 1, 2 or 3 (recommended setting: 0)
 Dwe_up/Dwe_down = WEBDELAY = 0, 1, 2 or 3 (recommended setting: 0)
 $(RCLK = 1/2 VRCLK)$

For more information please refer to the register descriptions for the GIO block in the μPD6121x User's Manual, document number S17532EEVxUM00.

Values for recommended setting of GAT = 2 RCLKs and ACTIVE_WAIT = 2 RCLKs

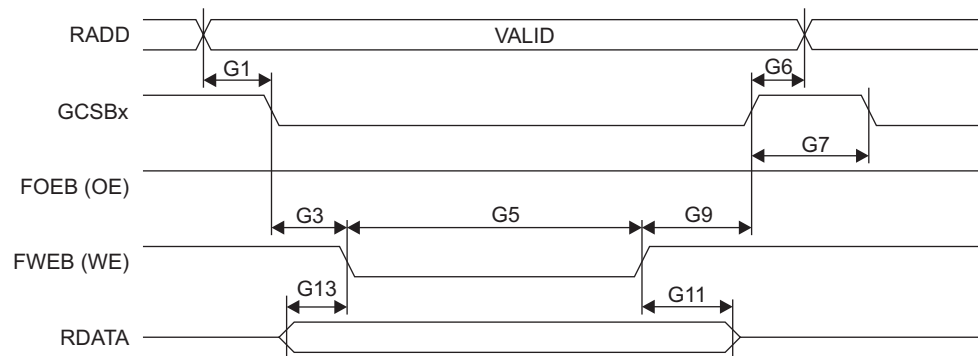
Symbol	Min	Typ	Max	Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
G1	16ns	—	—	G8	16ns	—	—	G15	21ns	—	—
G2	16ns	—	—	G9	16ns	—	—	G15A	—	—	90ns
G3	16ns	—	—	G10	0	—	—	G15B	21ns	—	—
G4	90ns	—	—	G11	37ns	—	—	G15C	0	—	78ns
G5	90ns	—	—	G12	21ns	—	—	G15D	21ns	—	—
G6	16ns	—	—	G13	37ns	—	—	G16	0	—	—
G7	58ns	—	—	G14	21ns	—	—	G17	0	—	—

Read timing, Intel mode, Non-Wait mode (GRDYEx = '1')



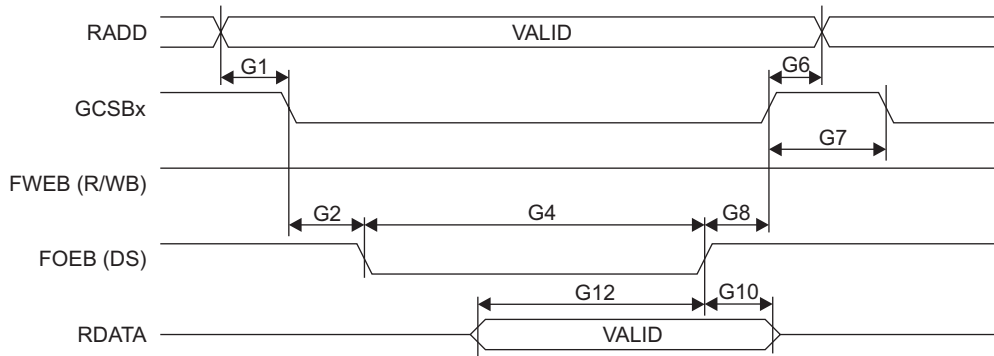
Timing_GIO_Int_Read_NW

Write timing, Intel mode, Non-Wait mode (GRDYEx = '1')



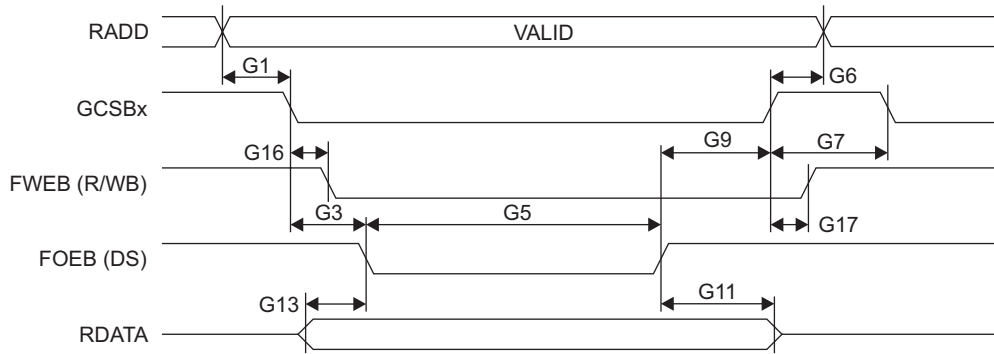
Timing_GIO_Int_Write_NW

Read timing, Motorola mode, Non-Wait mode (GRDYEx = '1')



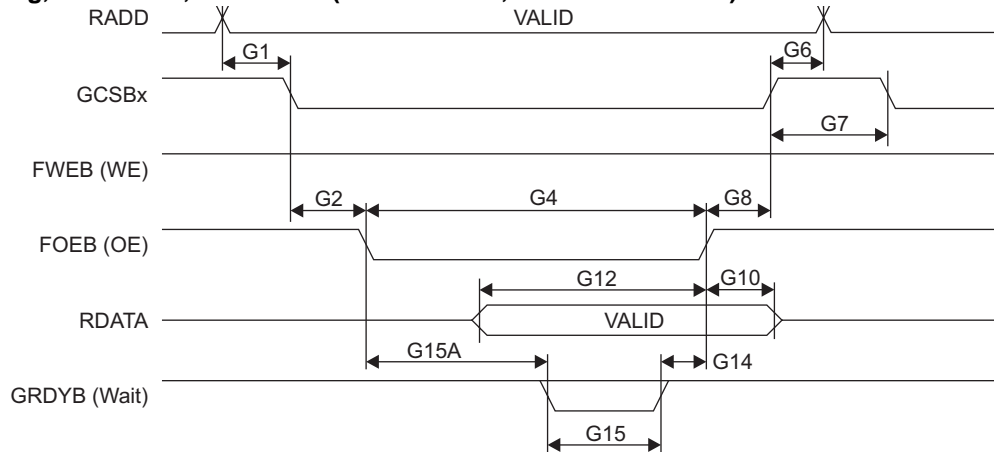
Timing_GIO_Mot_Read_NW

Write timing, Motorola mode, Non-Wait mode (GRDYEx = '1')



Timing_GIO_Mot_Write_NW

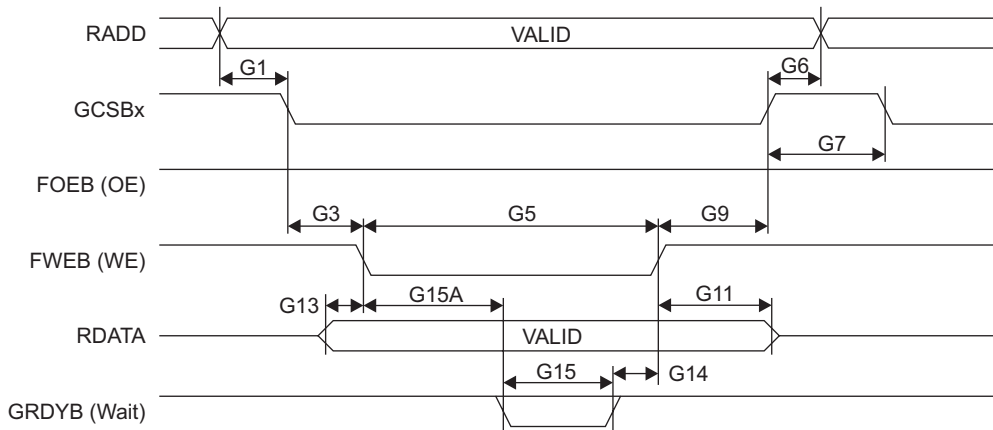
Read timing, Intel mode, Wait mode (GRDYEx = '0', GRDY/WAITx = '1')



Timing_GIO_Int_Read_W

Note: To extend the current bus transaction, GRDYBx must be asserted before G15A.

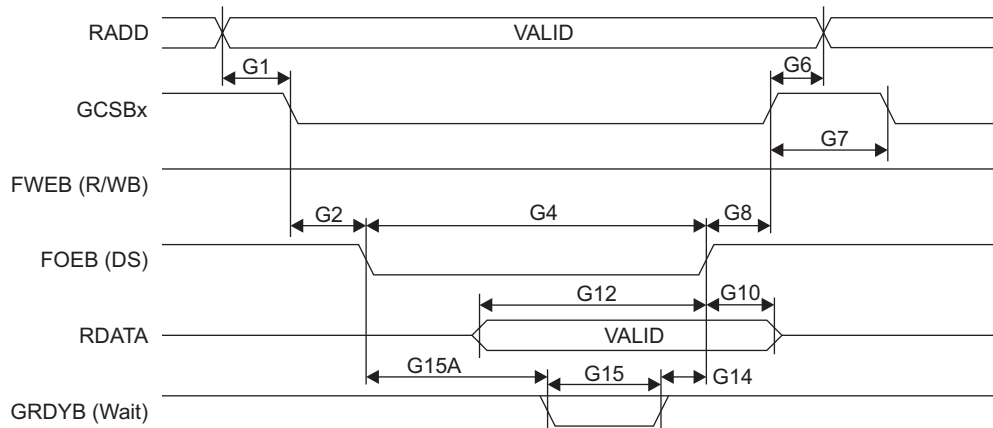
Write timing, Intel mode, Wait mode (GRDYEx = '0', GRDY/WAITx = '1')



Timing_GIO_Int_write_W

Note: To extend the current bus transaction, GRDYBx must be asserted before G15A.

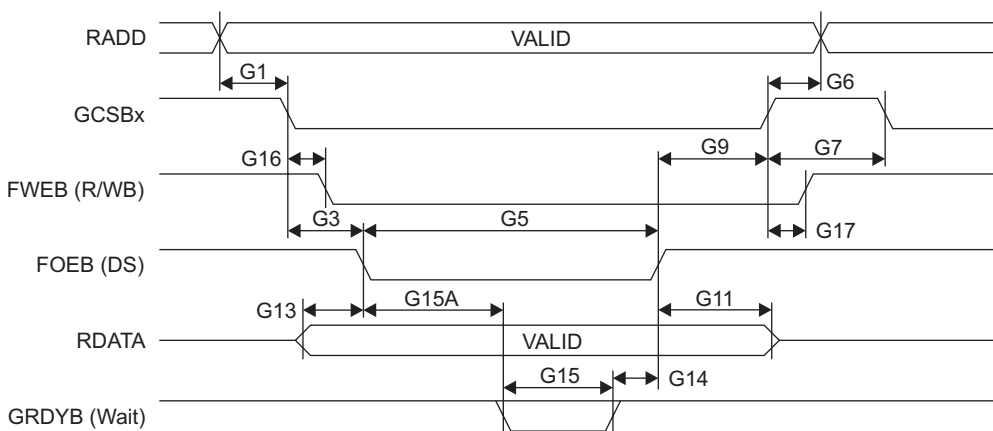
Read timing, Motorola mode, Wait mode (GRDYEx = '0', GRDY/WAITx = '1')



Timing_GIO_Mot_Read_W

Note: To extend the current bus transaction, GRDYBx must be asserted before G15A.

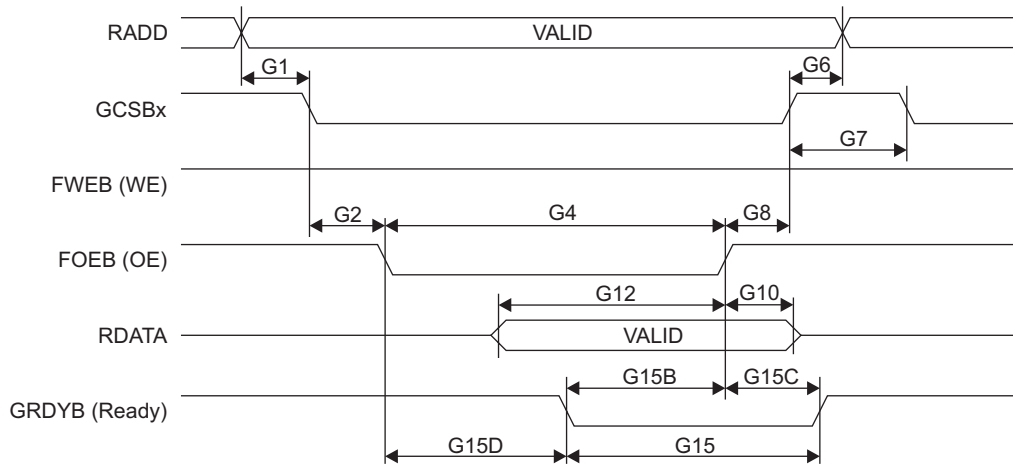
Write timing, Motorola mode, Wait mode (GRDYEx = '0', GRDY/WAITx = '1')



Timing_GIO_Mot_write_W

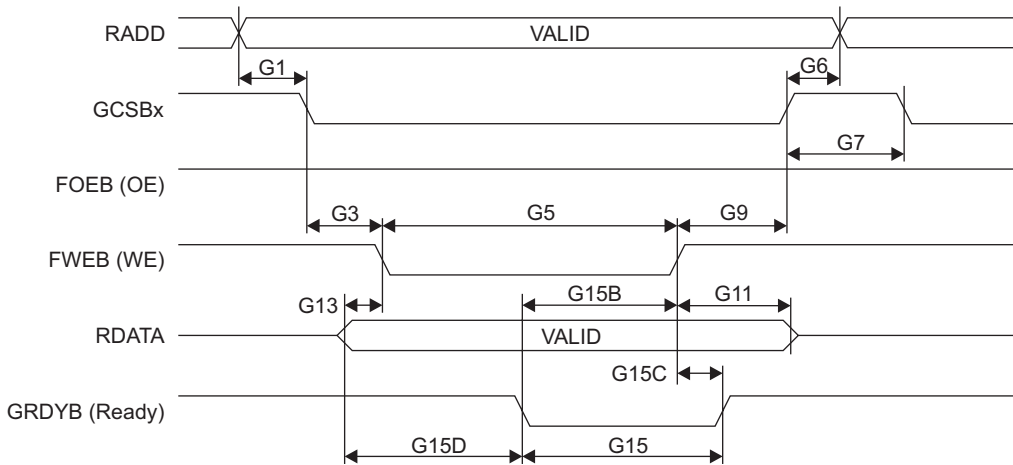
Note: To extend the current bus transaction, GRDYBx must be asserted before G15A.

Read timing, Intel mode, Ready mode (GRDYEx = '0', GRDY/WAITx = '0')



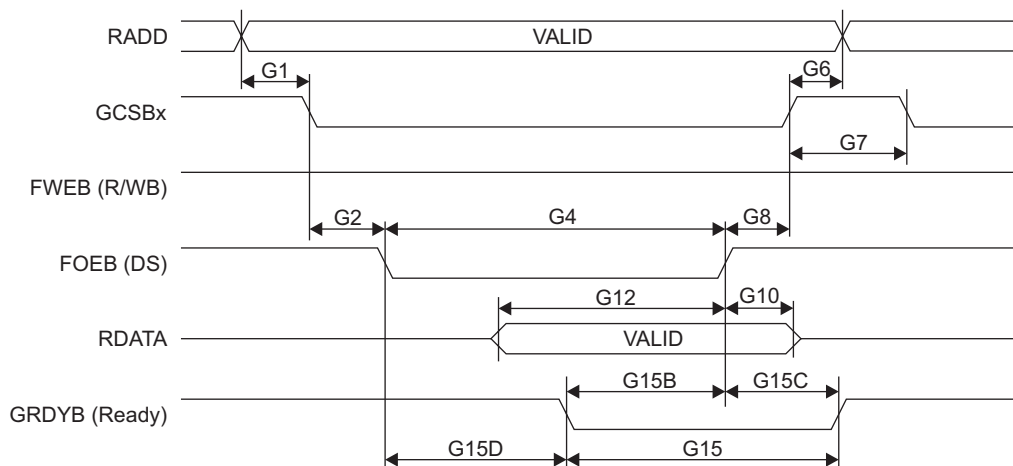
Timing_GIO_Int_Read_R

Write timing, Intel mode, Ready mode (GRDYEx = '0', GRDY/WAITx = '0')



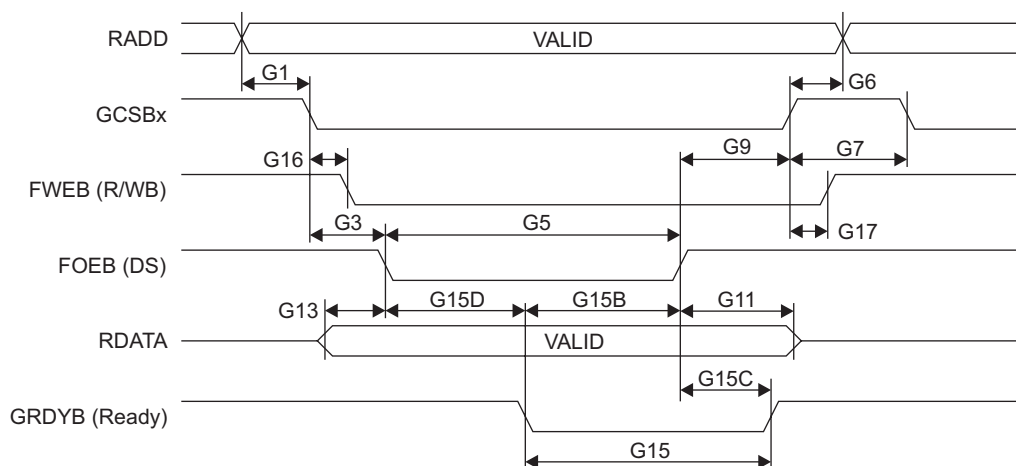
Timing_GIO_Int_write_R

Read timing, Motorola mode, Ready mode (GRDYEx = '0', GRDY/WAITx = '0')



Timing_GIO_Mo_Read_R

Write timing, Motorola mode, Ready mode (GRDYEx = '0', GRDY/WAITx = '0')



Timing_GIO_Mot_write_R

4.4.2 GIO Configured as a PCMCIA Interface

Symbol	Min	Typ	Max.	Unit
G1	$N*2T - T (-Dcs_down*2T)$	—	—	ns
G2	0	—	—	ns
G3	$N*2T - T (-Dcs_down*2T + Dwe_down*2T)$	—	—	ns
G4	$N*2T - T (-Dcs_down*2T)$	—	—	ns
G5	$N*6T - T (-Dcs_up*2T + Dcs_down*2T)$	—	—	ns
G6	—	—	$N*2T$	ns
G7	$N*2T - T (-Dcs_down*2T)$	—	—	ns
G8	0	—	—	ns
G9	—	—	$N*2T$	ns
G10	0	—	—	ns
G11	—	—	$(AW + 1)*2T - T (-Dwe_down*2T + Dwe_up*2T)$	ns
G12	0	—	—	ns
G13	0	—	—	ns
G14	$N*4T - T (-Dcs_down*2T)$	—	—	ns

Where:

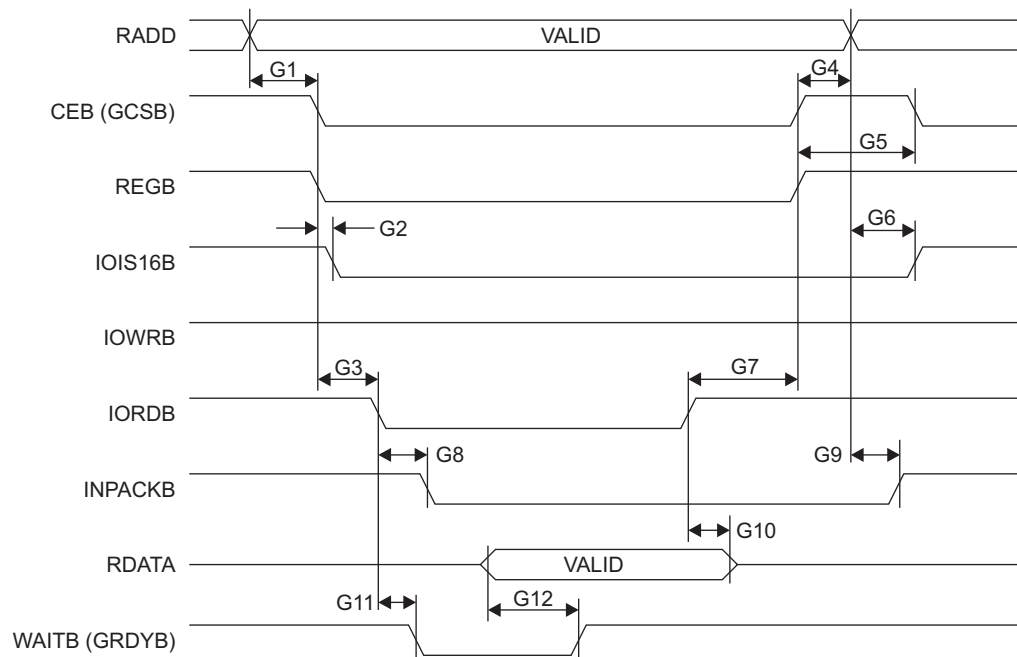
T = VRCLK period (5.34ns @ 187.3125MHz or 6.01ns @ 166.5MHz)
 N = GAT value in RCLK periods (programmable as 32, 2, 3, 4, 8, 16, 24 or 64)
 AW = ACTIVE_WAIT = 32, 2, 3, 4, 8, 16, 24 or 64 RCLKs
 Dcs_up/Dcs_down = CS0~4DELAY = 0, 1, 2 or 3 (recommended setting: 0)
 Doe_up/Doe_down = OEBDELAY = 0, 1, 2 or 3 (recommended setting: 0)
 Dwe_up/Dwe_down = WEBDELAY = 0, 1, 2 or 3 (recommended setting: 0)
 $(RCLK = 1/2 VRCLK)$

For more information please refer to the register descriptions for the GIO block in the μPD6121x User's Manual, document number S17532EEExVxUM00.

Values at recommended settings for a CPU clock of 187.3125MHz,
600ns mode, GAT = 8 RCLKs and ACTIVE_WAIT = 32 RCLKs

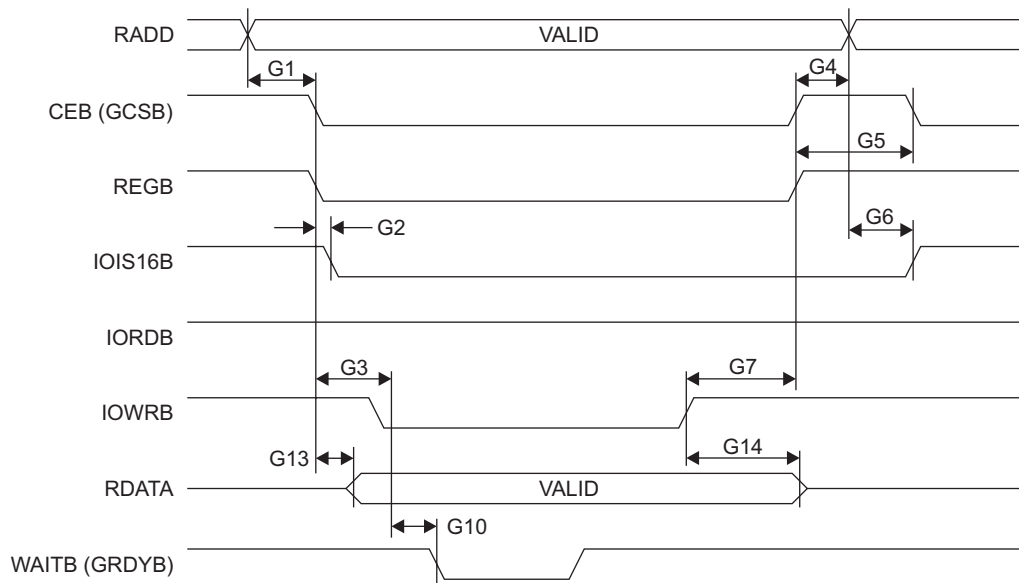
Symbol	Min	Typ	Max	Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
G1	80ns	—	—	G6	—	—	85ns	G11	—	—	352ns
G2	0	—	—	G7	80ns	—	—	G12	0	—	—
G3	80ns	—	—	G8	0	—	—	G13	0	—	—
G4	80ns	—	—	G9	—	—	85	G14	165ns	—	—
G5	250ns	—	—	G10	0	—	—				

PCMCIA Mode, I/O Access Read Timing



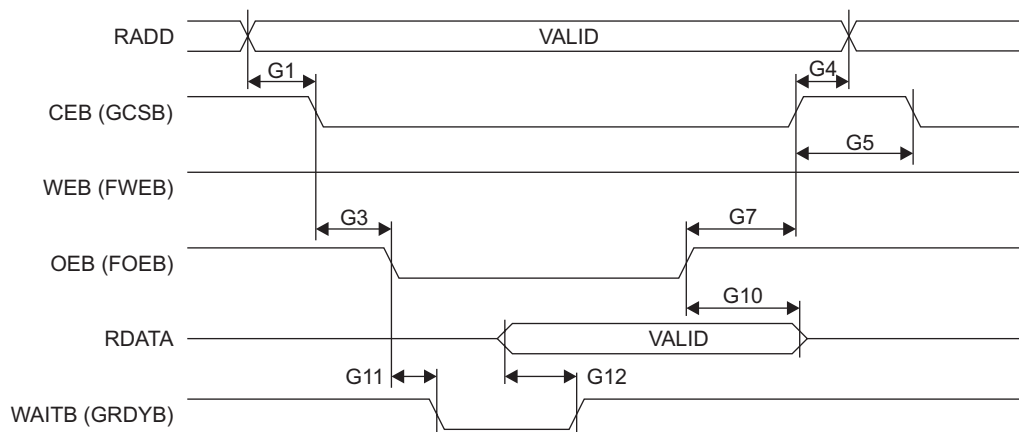
Timing_PCPCIA_IO_read

PCMCIA Mode, I/O Access Write Timing



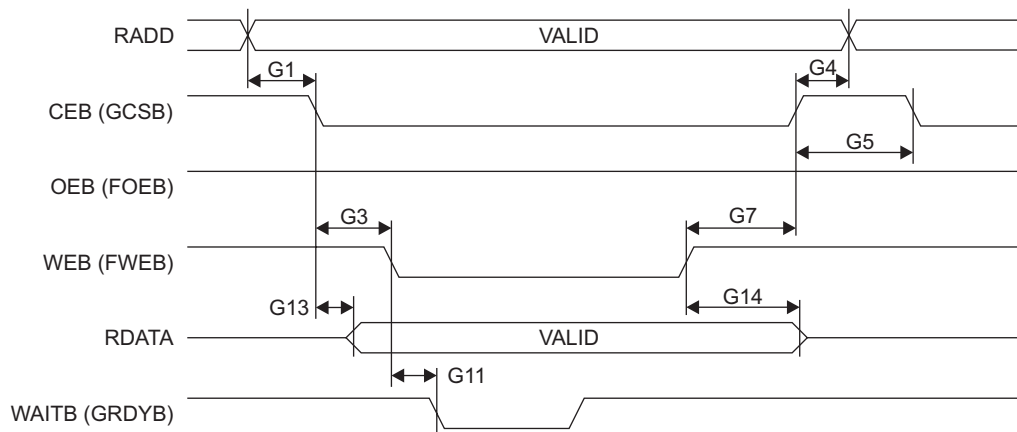
Timing_PCMCIA_IO_write

PCMCIA Mode, Memory Access Read Timing



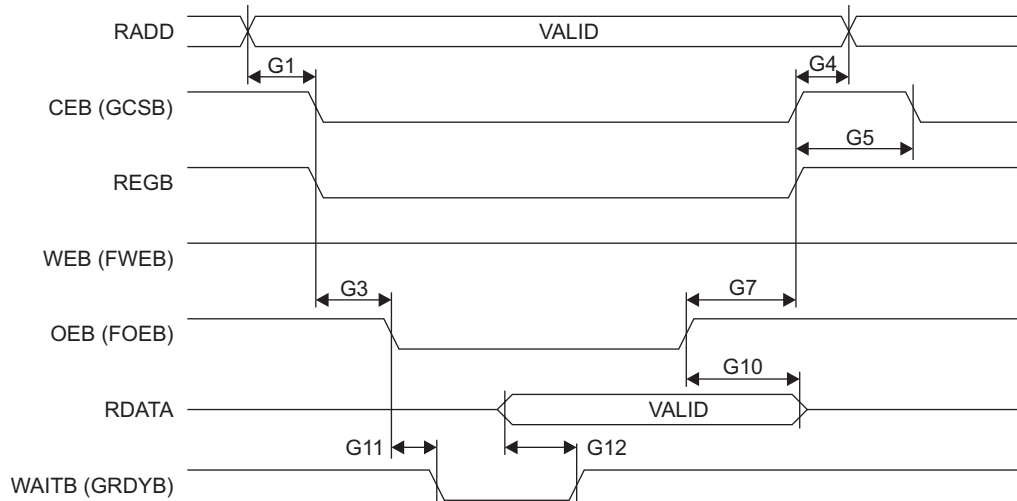
Timing_PCMCIA_mem_read

PCMCIA Mode, Memory Access Write Timing



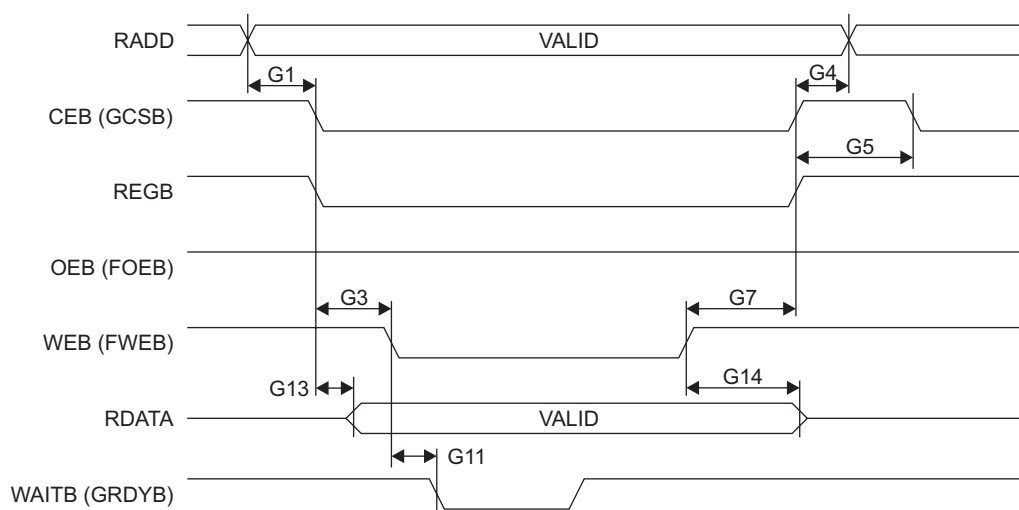
Timing_PCMCIA_mem_write

PCMCIA Mode, Attribute Memory Access Read Timing



Timing_PCMCIA_mem_attrib_read

PCMCIA Mode, Attribute Memory Access Write Timing

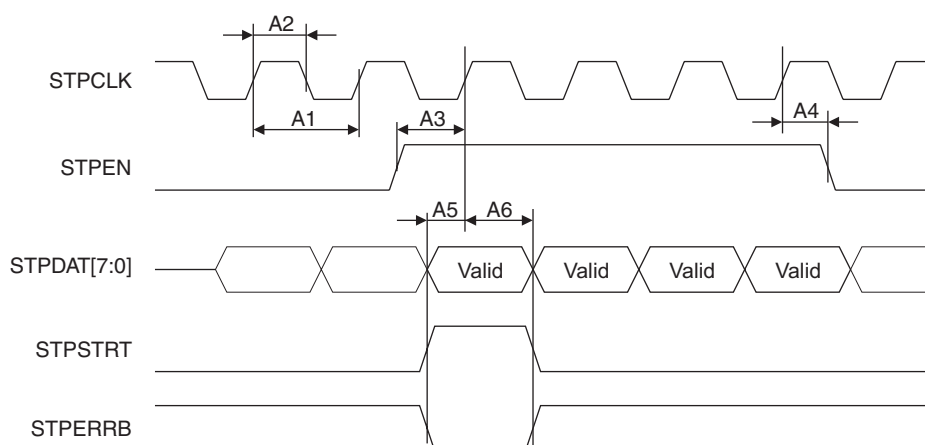


Timing_PCMCIA_mem_attr_write

4.5 Stream Interface

4.5.1 Parallel configuration

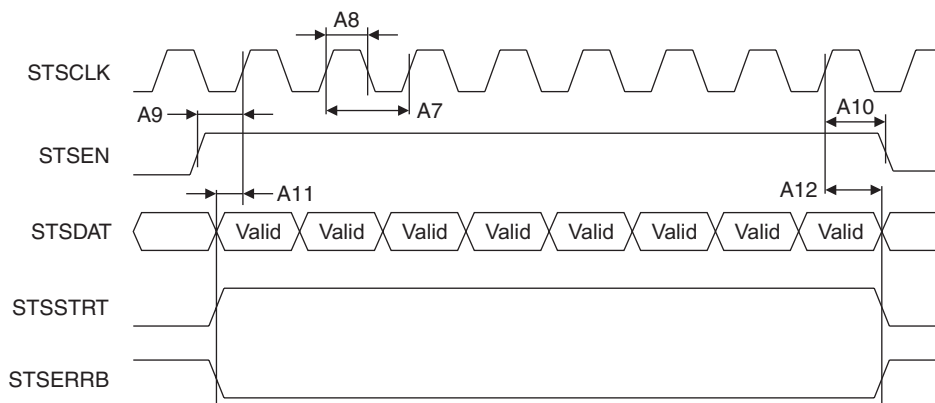
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
STPCLK frequency	A1	52	—	—	ns	
STPCLK high level width	A2	20	—	—	ns	
STPEN set-up time	A3	5	—	—	ns	
STPEN hold time	A4	5	—	—	ns	
Parallel Data-in set-up time	A5	5	—	—	ns	
Parallel Data-in hold time	A6	5	—	—	ns	



Timing_TS_Parallel

4.5.2 Serial configuration

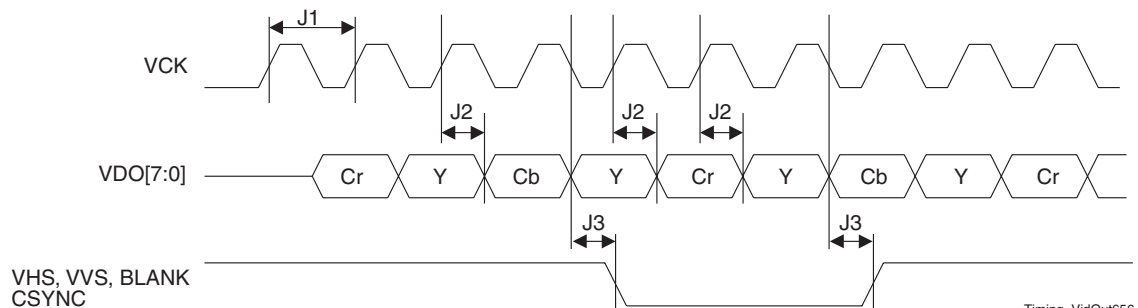
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
STSClk frequency	A7	10	–	–	ns	
STSClk high level width	A8	3.5	–	–	ns	
STSEN set-up time	A9	3.5	–	–	ns	
STSEN hold time	A10	3	–	–	ns	
Serial Data-in set-up time	A11	3	–	–	ns	
Serial Data-in hold time	A12	3	–	–	ns	



Timing_TS_Serial

4.6 Video Output – Digital

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
VCK frequency	J1	–	27	–	MHz	
Video Data output delay	J2	10	–	30	ns	
Video Sync Output Delay	J3	10	–	30	ns	

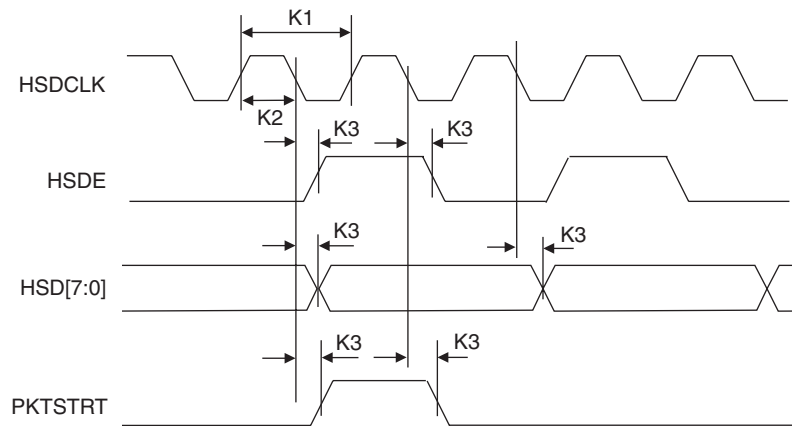


Timing_VidOut656

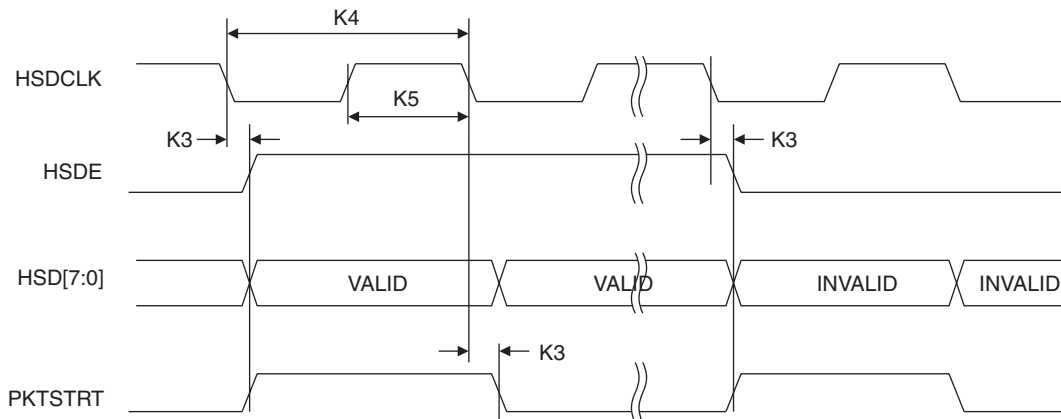
4.7 High Speed Data Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
HSDCLK frequency (type1)	K1	–	37	–	ns	
HSDCLK high level width (type1)	K2	–	18.5	–	ns	
HSDE/PKTSTRT/Data Output delay	K3	–5	–	+5	ns	
HSDCLK frequency (type2)	K4	70	–	–	ns	
HSDCLK high level width (type2)	K5	0.5 x K4	–	–	ns	

HSD Interface output timing – type 1



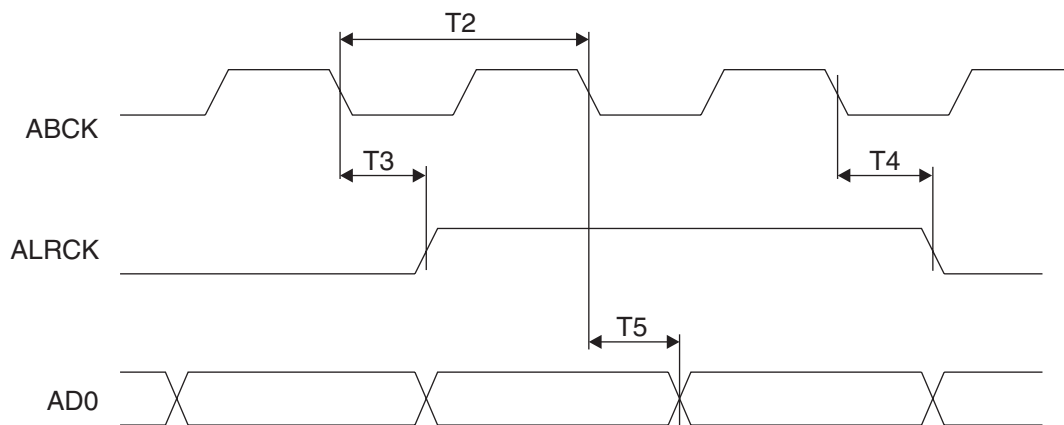
HSD Interface output timing – type 2



4.8 Audio Outputs

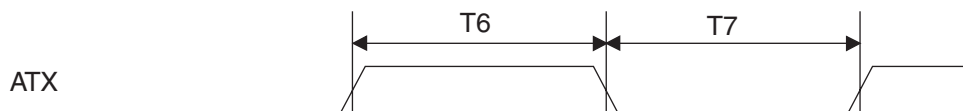
4.8.1 PCM Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
AMCK period	—	$1/(384 \cdot f_s)$	—	—	ns	
ABCK period	T2	$1/(64 \cdot f_s)$	—	—	ns	
ALRCK rising edge delay time from ABCK	T3	—	—	25	ns	
ALRCK falling edge delay time from ABCK	T4	—	—	25	ns	
ADO delay time from ABCK	T5	—	—	25	ns	



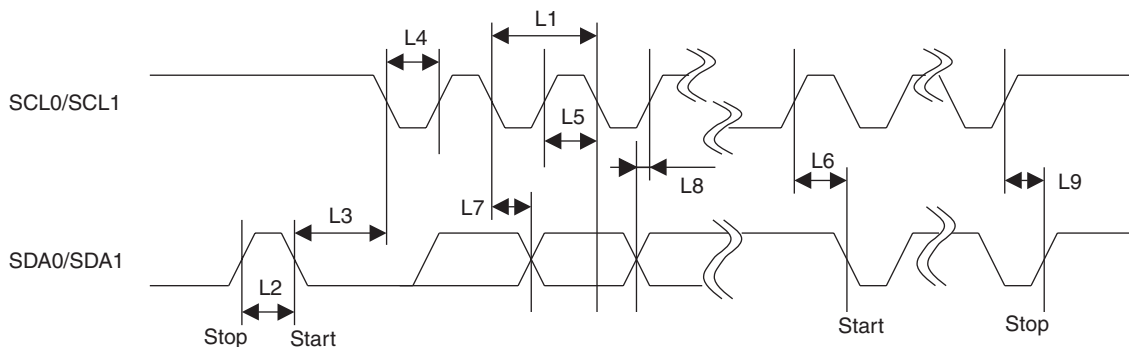
4.8.2 SPDIF Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
ATX pulse width high	T6	$1/(128 \cdot f_s)$	—	—	ns	
ATX pulse width low	T7	$1/(128 \cdot f_s)$	—	—	ns	



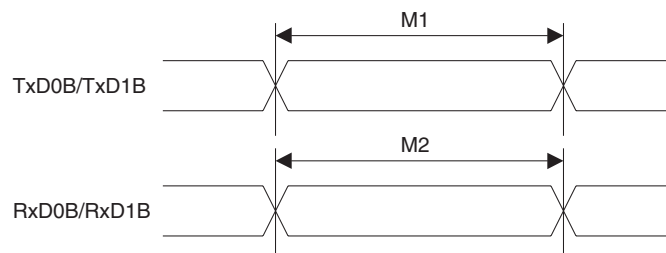
4.9 I²C Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
SCL0/1 clock frequency	L1	–	–	100	KHz	Normal
		–	–	400		Fast
Bus free time (Stop and Start)	L2	4.7	–	–	μs	Normal
		1.3	–	–		Fast
SCL0/1 hold time (on start)	L3	4.0	–	–	μs	Normal
		0.6	–	–		Fast
SCL0/1 low width	L4	4.7	–	–	μs	Normal
		1.3	–	–		Fast
SCL0/1 high width	L5	4.0	–	–	μs	Normal
		0.6	–	–		Fast
SCL0/1 set-up time (on start)	L6	4.7	–	–	μs	Normal
		0.6	–	–		Fast
SDA0/1 hold time	L7	5.0	–	–	μs	Normal
		0	–	–		Fast
SDA0/1 set-up time	L8	250	–	–	ns	Normal
		100	–	–		Fast
SCL0/1 set-up time	L9	4.0	–	–	μs	Normal
		0.6	–	–		Fast



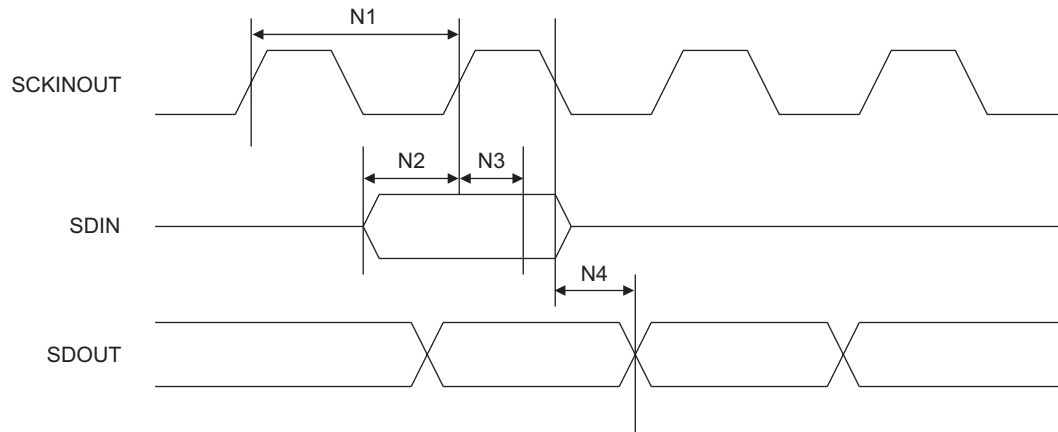
4.10 Fast UART Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
TxD0B/TxD1B pulse width	M1	6.3	–	–	μs	
RxD0B/RxD1B pulse width	M2	6.3	–	–	μs	



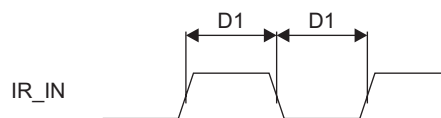
4.11 CSI (Clocked Serial Interface)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
SCKINOUT Cycle time	N1	0.868	–	–	μ s	
SDIN Data-in set-up time	N2	50	–	–	ns	
SDIN Data-in hold time	N3	65	–	–	ns	
SDOUT delay time	N4	–	–	65	ns	



4.12 IR Receiver Interface

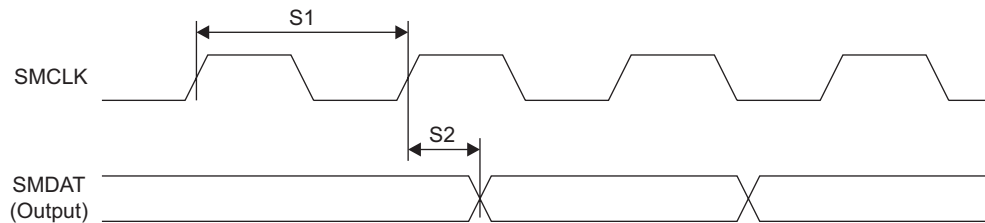
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input pulse width high or low	D1	50	–	–	μ s	



Timing_IR_in

4.13 Smart Card Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
SMCLK Clock frequency for Input	S1	–	–	20	MHz	
SMCLK Clock frequency for Output	S1	–	–	20	MHz	
Delay time SMCLK rising to SMDAT valid	S2	–	–	10	ns	

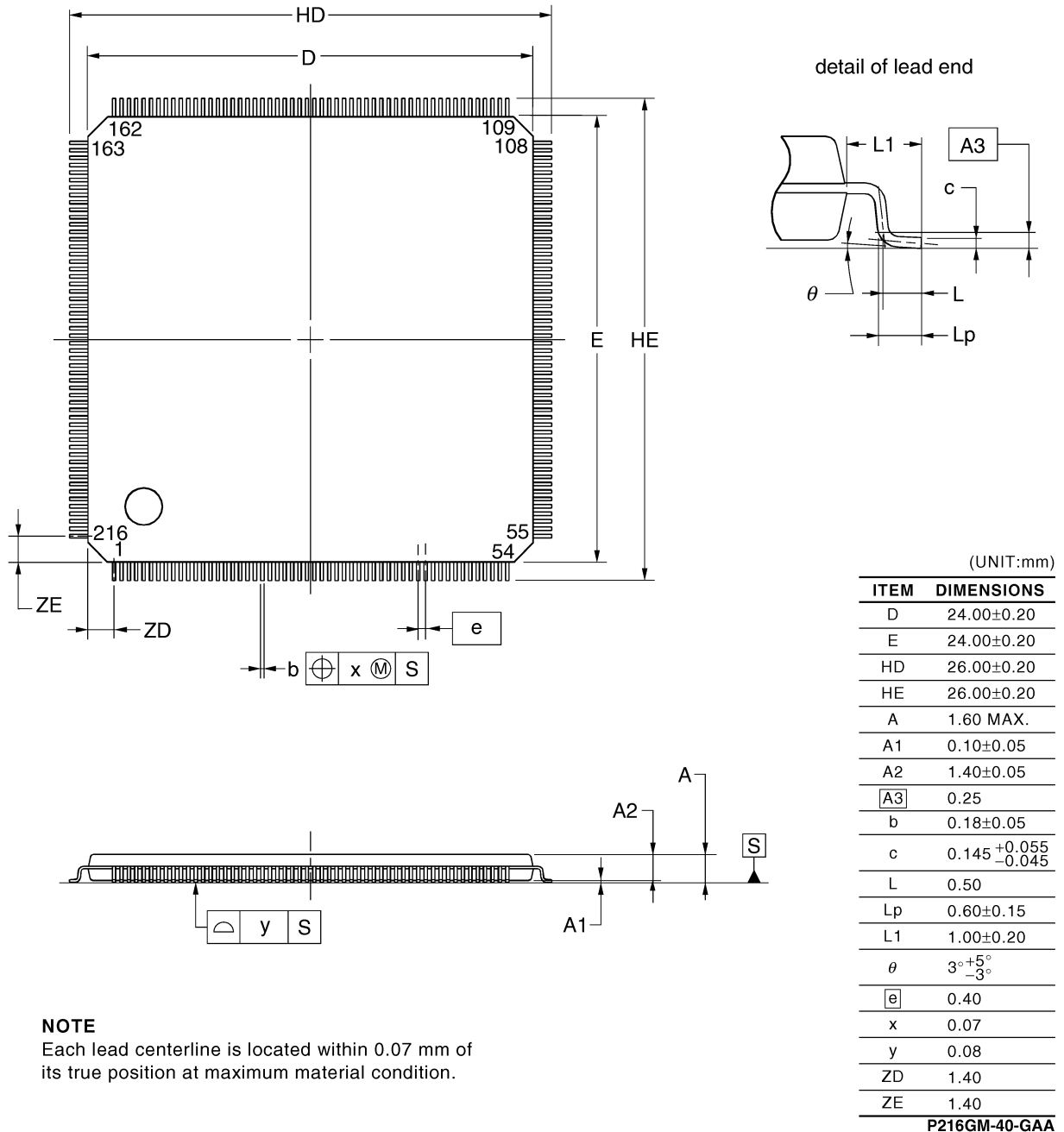


4.14 VCXO Interface

Use the same waveform as the system 27MHz clock shown in [section 4.1.1 on page 38](#).

5 PHYSICAL SPECIFICATIONS

5.1 Package Drawing: 216-pin Plastic LQFP (Fine Pitch) (24x24)



NOTE

Each lead centerline is located within 0.07 mm of its true position at maximum material condition.

5.2 Soldering Conditions

Full details of the soldering requirements and other background information on the device packages can be found in NEC's online resource here: <http://www.necel.com/pkg/en/index.html>.

REVISION HISTORY

Version	Date	Changes
1.0	2005-09-30	First release.
1.1	2005-11-01	No change to the technical information in this document. (Typographical error fixed and appendix updated.)
2.0	2006-03-07	<ul style="list-style-type: none"> • Corrections in the description of ‘ROM/GIO Interface’ on page 3. • On pages 3 and 8, the total address area for GIO was shown as “128MByte”. • Table 14 on page 18 ‘Optional Interface Conflicts’: details changed. • In table 34, ‘Global Pin List’, on page 28, the REF1 and RSET1 pins were shown interchanged. • In table 15 on page 19, pins FCSB1 and GCSB1 were shown with the wrong information in the ‘Pin no.’ and ‘Shared with’ columns. Also other changes in the ‘Shared with’ column. • Table 16 on page 20: changes in the ‘Shared with’ column. • In table 17 on page 21, the interface option was shown as ‘Boot option B’ only. • Tables 25 to 31, between page 25 and page 27, have been re-ordered to reflect a correction in the I/F option numbering shown in the tables. • In table 27 on page 26 the information in the ‘Pin no.’ and ‘Shared with’ columns was corrected. • In table 28 on page 26 the information in the ‘Pin no.’ and ‘Shared with’ columns was corrected and the reference to CAP/COM1~3 was deleted. • In several places in section 4.4.1, ‘Motorola and Intel Modes’, on page 45 and 46, the information in the timing tables was changed, “HCLK” was changed to “RCLK”, the values quoted for GAT and ACTIVE_WAIT in the notes under certain tables were changed and some timing diagrams were altered. • In section 4.4.2, ‘GIO Configured as a PCMCIA Interface’, on page 50, changes were made to the tables and notes at the start of the section but the timing diagrams are unchanged. • Section 4.11, ‘CSI (Clocked Serial Interface), on page 59: value for N1 was 1.18μs • Section 4.1.2, ‘Reset and Strap Input Timing’, on page 38: “Q6” removed from diagram. • Section 5.1: package drawing updated. • Table 35 on page 30: deleted pin Code 6. • Table 5 on page 15: added pin “CLK27OUT”. • Changed timing diagram and values for ‘IR Receiver Interface’ on page 59.
2.1	2006-06-30	<ul style="list-style-type: none"> • Soldering Conditions, section 5.2 on page 61: web page URL changed. • Ordering numbers on front page changed to add “-A” and “Pb-free”. • “EMMA2SL” added to front page, EMMA trademark reference added to back page and doc templates updated.
2.2	2006-09-06	Section 3.6, ‘DAC Characteristics – Analog Video Outputs’, on page 32 : changed the value of “K” below the table from 3.1 to 4.55.
2.3	2006-11-01	Section 2.2.2, ‘Strap Pin Settings’, on page 14 : changed the options for ‘RADD[22:21]’ on page 14 .
2.4	2007-01-08	<p>Section 2: entire section rearranged for improved clarity.</p> <p>Section 3 on page 31: notes added regarding <i>Absolute Maximum Ratings</i> and <i>Recommended Operating Range</i>.</p>

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including workbench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

EMMA is a trademark or registered trademark of NEC Electronics in Japan and other countries.

MIPS32, 4KEc and 4KEm are trademarks of MIPS Technologies Inc. in the USA and other countries.

Macrovision is a trademark of Macrovision Corporation in the USA and other countries.

All other trademarks or registered trademarks are the property of their respective owners.

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
 - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
 - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
 - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
 - While NEC Corporation has been making continuous effort to enhance there liability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
 - NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8