



## Ordering Information

| Model Number | Package      | Operating Temperature |
|--------------|--------------|-----------------------|
| CX24138      | 208-pin MQFP |                       |

## Revision History

| Revision | Date               | Description                                                                                                                                                  |
|----------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| p1       | September 28, 2004 | Initial release                                                                                                                                              |
| p2       | November 2, 2004   | Second release. In Table 7, Function Comparison between CX24138 and CX2414X, External Bus Interface row, adds sentence about IO bus control signal IO_READY. |

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# Contents

|                                                                           |    |
|---------------------------------------------------------------------------|----|
| Figures .....                                                             | 5  |
| Tables .....                                                              | 7  |
| 1 CX24138 Product Description .....                                       | 9  |
| 1.1 CX24138 Features .....                                                | 11 |
| 1.2 Functional Overview .....                                             | 12 |
| 1.2.1 Transport/PES Stream De-Multiplexing .....                          | 12 |
| 1.2.2 Video Decoding .....                                                | 13 |
| 1.2.3 Audio Decoding and PCM I/O .....                                    | 13 |
| 1.2.4 Video/Graphics Display .....                                        | 13 |
| 1.2.5 TV Encoder .....                                                    | 13 |
| 1.2.6 2D Graphics Engine .....                                            | 14 |
| 1.2.7 System CPU Core .....                                               | 14 |
| 1.2.8 SDRAM Memory Controller .....                                       | 15 |
| 1.2.9 Peripheral I/O Controllers .....                                    | 15 |
| 1.2.10 System I/O Bus Controller .....                                    | 15 |
| 1.3 CX24138 Pinout .....                                                  | 16 |
| 1.3.1 208 MQFP Package Drawing .....                                      | 16 |
| 1.3.2 CX24138 Pinlist .....                                               | 20 |
| 1.4 Configuration Pin Use .....                                           | 33 |
| 1.4.1 CX24138 Configuration Register—Hardware Initialization .....        | 34 |
| 1.4.1.1 Hardware Initialization Bits Not Used on Production Designs ..... | 34 |
| 1.4.1.2 Hardware Initialization Bits Required for Customer Designs .....  | 34 |
| 2 Register Index .....                                                    | 37 |
| 3 Comparison between CX24138 and CX2414X .....                            | 57 |
| 3.1 Function Comparison .....                                             | 57 |
| 3.2 Register Definition and Table .....                                   | 59 |
| 3.2.1 Interrupt Controller .....                                          | 59 |
| 3.2.2 High-Speed Data Port .....                                          | 62 |
| 3.2.3 Infrared Remote Control Interface .....                             | 66 |
| 3.2.4 I/O Interface Register Descriptions .....                           | 72 |
| 3.2.5 GPIO .....                                                          | 75 |
| 3.2.6 PCM Audio I/O Controller .....                                      | 76 |
| 3.2.7 DTDC CPU Interface .....                                            | 78 |

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# Figures

|           |                                     |    |
|-----------|-------------------------------------|----|
| Figure 1. | CX24138 Block Diagram .....         | 9  |
| Figure 2. | CX24138 Detailed Block Diagram..... | 10 |
| Figure 3. | 208-Pin MQFP Package Drawing .....  | 17 |
| Figure 4. | CX24138 Pinout .....                | 18 |

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# Tables

|           |                                                                    |    |
|-----------|--------------------------------------------------------------------|----|
| Table 1.  | 208-Pin MQFP Size Parameters . . . . .                             | 19 |
| Table 2.  | CX24138 Pinlist . . . . .                                          | 21 |
| Table 3.  | CX24138 I/O Mode Pin Table . . . . .                               | 31 |
| Table 4.  | Unused Hardware Configuration Bits . . . . .                       | 34 |
| Table 5.  | Required Hardware Configuration Bits . . . . .                     | 35 |
| Table 6.  | CX24138 Register Index . . . . .                                   | 37 |
| Table 7.  | Function Comparison between CX24138 and CX2414X . . . . .          | 57 |
| Table 8.  | Top-Level Interrupt Status Positions Bit Contents . . . . .        | 59 |
| Table 9.  | Expansion Positions Bit Contents . . . . .                         | 61 |
| Table 10. | HSDP 0 Control Register Bit Definitions . . . . .                  | 62 |
| Table 11. | Demux Input Selection Register Bit Definitions . . . . .           | 63 |
| Table 12. | Transport Stream Packet Control Register Bit Definitions . . . . . | 64 |
| Table 13. | Transport Stream Error Status Register Bit Definitions . . . . .   | 65 |
| Table 14. | HSDP 0 Clock Control Register Bit Definitions . . . . .            | 65 |
| Table 15. | IR Control Bit Descriptions . . . . .                              | 66 |
| Table 16. | Status Bit Descriptions . . . . .                                  | 68 |
| Table 17. | Interrupt Enable Register Bit Descriptions . . . . .               | 70 |
| Table 18. | FIFO Register Bit-Field Descriptions . . . . .                     | 71 |
| Table 19. | ROM Descriptor 0 Register Bit Definitions . . . . .                | 72 |
| Table 20. | ISA Descriptor 4 through 7 Register Bit Definitions . . . . .      | 73 |
| Table 21. | ROM Mode Register Bit Definitions . . . . .                        | 74 |
| Table 22. | Available GPIO Pins . . . . .                                      | 75 |
| Table 23. | Channel Control Register Bit Definitions . . . . .                 | 76 |
| Table 24. | Audio Interface Register Pin Descriptions . . . . .                | 77 |
| Table 25. | CONTROL1 Register Bit Definitions . . . . .                        | 78 |
| Table 26. | Decoder Status Register Bit Definitions . . . . .                  | 80 |

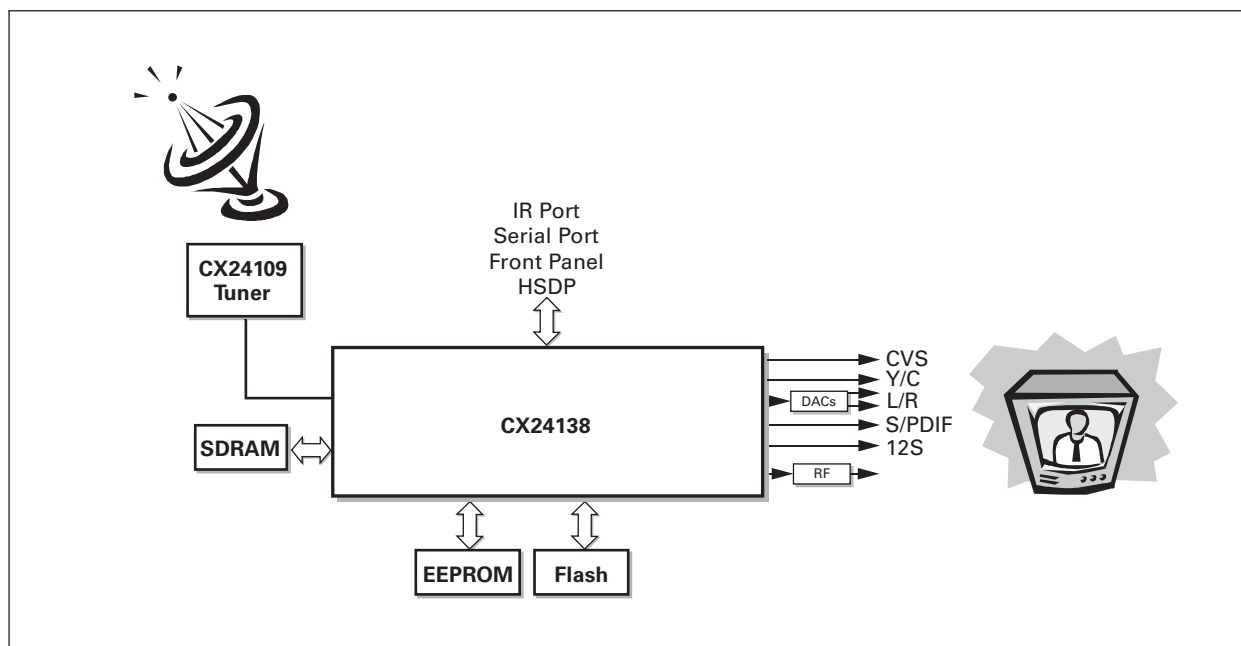
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# CX24138 Product Description

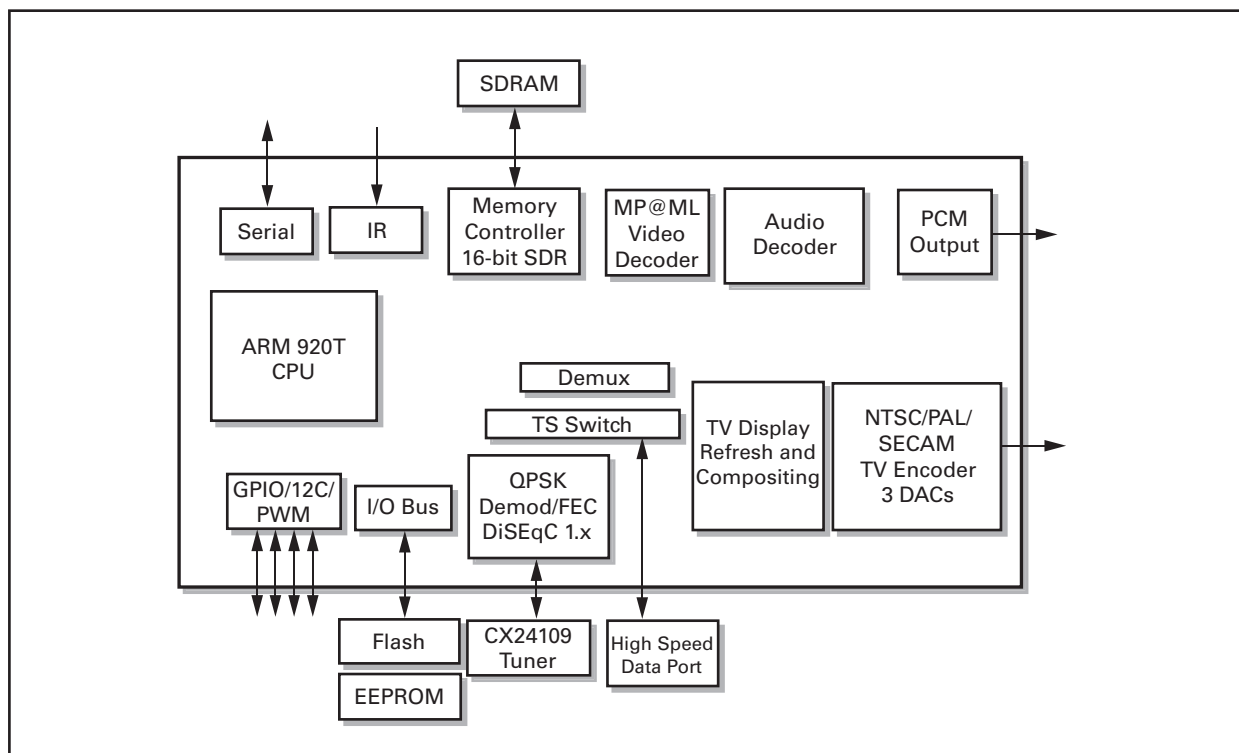
Conexant's CX24138 is a highly integrated, single IC, MPEG-2/DVB compliant, receiver/decoder solution for digital satellite STBs. The CX24138 combines an MP@ML MPEG-2 video decoder, a digital audio decoder, a programmable transport stream de-multiplexer, an advanced graphics/OSD display controller, a QPSK demodulator/FEC unit and a TV encoder with a high-performance, embedded 32-bit ARM920T RISC processor and integrated peripheral I/O ports. The CX24138 compliments the existing MPEG-2/DVB receiver/decoder units supplied by Conexant by providing the functionality in a low-cost MQFP package.

Combined with a Conexant IC tuner and memory as shown in [Figure 1](#), the CX24138 offers a complete, low-cost, IC solution for digital satellite IRDs. A detailed block diagram of the CX24138 is shown in [Figure 2](#).

**Figure 1. CX24138 Block Diagram**



102511\_001

**Figure 2. CX24138 Detailed Block Diagram**

102511\_002

The CX24138 incorporates an advanced video and graphics display controller to enable a rich navigation/user interface. The CX24138 can resize and mix still video images with graphics and MPEG-2 decoded video to create a visual interface, which blends a digital TV picture with graphics, video stills and OSD images.

The CX24138 integrates a high-performance, 133-MHz, Synchronous Dynamic Random Access Memory (SDRAM) memory controller supporting a unified memory architecture. This single SDRAM memory system is used to support the requirements of the embedded processor, the MPEG-2 A/V decoder, the transport de-multiplexers, and the graphics OSD. This eliminates the need for multiple, discrete memory subsystems and provides optimal flexibility to take advantage of the various features and performance of MPEG decoders, graphics, operating systems, and applications software.

The CX24138 has been specifically tailored to meet the H/W requirements of a low-cost satellite STB via integration of a QPSK demodulator FEC unit.

**NOTE:**

In this document, the descriptions of CX2414X are as documented in *CX2414X Interactive TV Decoder IC Manual*, document number 102210B, June 2004.

## 1.1 CX24138 Features

- ◆ MPEG-2 MP@ML Video Decoder
  - Decodes image sizes up to 720x480 @30fps NTSC & 720x576 @25fps PAL
  - Supports MPEG-1 video decoding
  - Up-sampling and filtering of low resolution video modes to full CCIR601 picture size
  - 14:9, 16:9 & 20:9 image aspect ratio support through pan/scan or letter boxing
  - Supports 3:2 pull-down of 24fps video sequence
- ◆ MPEG-1, MPEG-2 Audio Decoder
  - Decodes Layer I & II (MUSICAM) ISO 11172
  - Supports stereo down-mix extraction from multi-channel MPEG-2 source
  - Up to 20-bit LPCM 2-channel output in I2S or left justified serial formats
  - Supports sample rates of 16, 22.05, 24, 32, 44.1, 48kHz
  - Supports bit rates up to 640kbps
  - Supports external base-band & over-sampling DACs
  - Automatic error concealment
  - A/V synchronization using PTS & STC
  - Integrated PLLs generate all required audio clocks from external low-cost crystal oscillator
- ◆ Multi-Standard, Multi-Stream Transport De-multiplexing
  - Parses MPEG-2/DVB/DirecTV transport or PES streams
  - Supports up to 72.5Mbps sustained data rate
  - Filters up to 40 PIDs per stream
  - 48 PSI and SI table section filter support
  - Robust MPEG-2 transport packet framing & synchronization, error recovery & packet loss handling
  - PCR/SCR timing recovery
  - Extracts CC or WST teletext bitstream
  - Full duplex, baseband transport stream I/O via high-speed data port
  - Internal multiplexing/routing of input transport streams from demod and high-speed data port
- ◆ 32-bit ARM920T Main System CPU
  - 146 Dhrystone 2.1 MIPS at 133 MHz
  - 16KB data cache, 16KB instruction cache
  - WinCE compatible MMU
  - 133 MHz, 16-bit SDRAM controller supporting required 4/8 MB of unified memory using 16/32/64Mb SDRAM.
- ◆ Analog Video Outputs
  - CVBS, RGB, S-video supported via 3 video DACs.
- ◆ OSD/Graphics Plane Display
  - Supports 16bpp non-palettized RGB/YCrCb graphics with alpha
  - 4, 8 bpp palettized graphics with alpha
  - High quality anti-flicker filtering of RGB OSD
  - RGB to YCrCb color conversion
  - Square pixel RGB graphics OSD aspect ratio compensation
  - Multi-region OSD support
  - 8-bit alpha blending on video for translucent OSD overlay
- ◆ Video Plane Display
  - Single or dual 4:2:0 MPEG video plane display
  - MPEG video downscaling for picture-in-graphics
  - Video image blend with background color
  - MPEG/JPEG 4:2:0 still image decoding, scaling and compositing/blending

- with tile/wipe effects
- ◆ Advanced 2D Graphics Accelerator
  - Supports compositing of multiple overlapping graphics surfaces in frame buffer via alphablend
  - Bitblt, line draw, color fill, textblt, color conversion, ROPs rendering acceleration
  - Supports graphics rendering engine command queue
- ◆ Peripheral I/O Interfaces
  - 16-bit I/O bus for ROM, flash, H/W modem
  - Generic IR remote control receiver
  - UART, I2C ports/GPIO/PWM
  - Numerous 5 V tolerant I/O pins
- ◆ Miscellaneous System Components
  - Interrupt controllers, timers, real time clock, power managements
  - On-chip clock generation using internal PLL
- ◆ Package/Power Supply
  - 27 mm MQFP

## 1.2 Functional Overview

### 1.2.1 Transport/PES Stream De-Multiplexing

The CX24138 supports one serial baseband transport stream I/O port. The transport stream demultiplexer unit can source its transport stream input from this transport stream port or from the integrated QPSK demodulator FEC block in the CX24138.

The CX24138 is available with an integrated QPSK demodulator FEC. The transport stream demultiplexer contains both a DVB common descrambling module and a DES ECB/CBC mode decryption module to perform transport or PES payload descrambling. The demultiplexer's embedded microprocessor retrieves ECMs and EMMs from the PSI/SI data and obtains control keys from the EMMs.

After descrambling and error recovery, the Transport Stream De-multiplexer performs transport header parsing, PES header parsing and PSI/SI header parsing and extraction. The PID filters pass through the selected video and audio data, the PCR, as well as up to 30 other user-defined packet streams. The Program Clock Reference is sent to a system timing generator while the other streams are temporarily stored in local memory. Video and Audio streams are automatically detected and sent to the MPEG-2 Video Decoder and MPEG Audio Digital Decoder encoded data buffers in SDRAM respectively, while user data streams (including teletext and subtitling) must be taken out of local SDRAM memory by the embedded ARM CPU. The transport demultiplexer can also output partially processed transport packets (any combination of PID filtering, descrambling and section filtering) to the baseband transport stream output port.

A system timing generator uses a single external crystal and on-chip PLLs to provide all required clock signals for A/V decoding, memory controller, CPU, display controller, audio controller, clock recovery functions.

## 1.2.2 Video Decoding

The MPEG video decoder module decodes MPEG-1 and MPEG-2 MP@ML video bitstreams at bit-rates up to 15Mbit/sec. A range of video picture resolutions are supported including: 720x576, 544x576, 480x576, 352x576, 352x288, 720x480, 544x480, 480x480, 352x480, 352x240.

Up-sampling to CCIR601 for the low resolution picture modes is implemented using a high-performance two dimensional interpolation filter. Error concealment is applied down to the slice level.

## 1.2.3 Audio Decoding and PCM I/O

CX24138 supports MPEG-1 single channel, dual channel, joint-stereo and stereo modes. MPEG-2 backward compatible bit-streams are also supported at both half and full sample rates. MPEG audio can be decoded with or without de-emphasis.

## 1.2.4 Video/Graphics Display

The Video/Graphics display controller manages display refresh for all image sources including MPEG video, still plane video and graphics. up to 5 independent image hardware planes are supported including cursor, graphics/OSD, MPEG video, still plane video, plane and background color. Graphics is displayed as an overlay of up to 16 bits per pixel on top of the video picture. The graphics OSD can be generated as a full screen OSD or can be implemented as a multi-region OSD with each region having a separate palette context limited to one region/palette per display line. The 256 color palette can be configured as four independent 16-color palettes to provide four plane OSD capability on the same display line. The graphics plane can be both vertically filtered to eliminate flicker and horizontally scaled to correct for square pixel aspect ratio distortion before mixing with video.

The MPEG and still plane video picture may be arbitrarily down-scaled down to a factor of 1/4 independently in both X and Y dimensions using a high-quality 2 dimensional interpolation filter. MPEG video can be mixed with the still plane video source on a region basis prior to mixing with the graphics plane. The still plane video buffer contains a 4:2:0 or 4:2:2 image which will typically be a decoded MPEG/JPEG still image. Graphics is mixed with video using an alpha blend and a scaled video picture can be embedded inside a full screen graphics image or it may be an overlay on top of a second, full screen video picture. Any arbitrary rectangular region of the decoded MPEG still plane video picture can be cropped and zoomed up to fill an entire CCIR601 picture size. Wipe and tiling affects are also supported for the still plane.

The second OSD plane can be blended with MPEG/still video and the resulting image can then be blended with the primary graphics/OSD plane.

## 1.2.5 TV Encoder

The TV Encoder module is a highly programmable digital composite video encoder supporting worldwide broadcast standards. The TV Encoder module acts as the timing master for the display refresh engine generating ITU-R BT.601 timing.

The TV Encoder has three 10-bit current-output video DACs. The TV encoder is specifically designed for video systems requiring the generation of high-quality composite, Y/C (S-Video), and component YPrPb or RGB (SCART) video signals. The connection status of each DAC can be dynamically monitored. Low power options include sleep mode, individual DAC disable, low voltage DAC supply voltage, and reduced current DAC operation when driving high impedance loads. An enhanced luminance upsampling filter provides a narrow transition region and a low stopband. Programmable luminance sharpness filters provide 0, 1, 2, and 3.5 dB peaking options at higher video frequencies, and four reduction filters are added for smoothed step response. To reduce the complexity of the required reconstruction filter, 2x upsampling is implemented. The TV Encoder provides support for Closed Captioning (CC) and Extended Data Services (XDS), Teletext (WST system B), Copy Generation Management System (CGMS), VARIS-II, and Wide Screen Signaling (WSS). It can also generate Macrovision 7.1 anti-copy signaling. See the CX24138 Interactive TV Decoder Part Number Guide for details regarding which CX24138 devices support Macrovision copy protection.

## 1.2.6 2D Graphics Engine

The 2D Graphics Engine performs Bit BLTs, rectangle fill, and line draw. The command interface is through a 32 entry deep command queue, allowing independent operation of the graphics engine. Multiple rendering commands and rendering context changes can be stored by the host processor, as long as space is available in the queue. Multiple pixel formats are supported in 8 and 16 bit per pixel widths. Bit BLTs may be full color in any of the available pixel formats. Color expansion from a mono source to any of the pixel formats is also supported.

Composition of rendered data into a destination image is supported with raster operations (ROP) or alpha blending. Sixteen standard logical operations are provided to combine the rendered pixel with the destination pixel. Alpha blending allows multiple graphic surfaces to be combined into a single image buffer. The alpha value is selected to be the source image alpha, the destination image alpha or a fixed alpha value.

## 1.2.7 System CPU Core

The embedded ARM920T CPU core provides complete system level host set top box processor functions. This 32-bit RISC processor provides up to 146 MIPS integer CPU performance.

The ARM9 core is a high-performance, power-efficient 32-bit RISC processor. The core features a five-stage pipeline, Harvard buses, Thumb extension and full debug access to all programmer's model states. The Thumb code compression extension delivers 32-bit RISC performance at 16-bit system costs through the efficient use of a second, compressed set of 16-bit instructions, which reduces memory use by a third.

The ARM920T includes separate 16KB instruction and data caches to the two memory data buses for reduced access time to both instructions and data. The ARM920T incorporates two coprocessors CP14 and CP15. CP14 allows software access to the debug communications channel. The system control coprocessor, CP15, is used to configure and control the caches, MMU, protection system, clocking and other system options such as big/little-endian operation. The

ARM920T implements an enhanced ARM architecture v4 MMU to provide translation and access permission checks for instruction and data addresses. The MMU page tables that reside in main memory describe the virtual to physical mapping, access permissions and cache and write buffer configuration. These are created by the operating system and accessed automatically by the MMU hardware whenever an access causes a TLB miss.

## 1.2.8 SDRAM Memory Controller

All external DRAM system requirements are supported through a single, physical SDRAM memory system. This is organized as one rank supporting x16 memory device organization.

All standard 16Mb, 64Mb, 128Mb & 256Mb SDRAM device densities can be used to configure memory buffer sizes of 4, 8, 12, 16, 20, 24, and 32 MB SDRAM. Memory speeds up to 133 Mhz are supported.

## 1.2.9 Peripheral I/O Controllers

A complete set of user control and peripheral device interfaces are integrated into the system, providing IR receiving, I2C, serial, and GPIO ports.

The generic functionality for an IR remote receiver interface is provided in hardware with the IR protocol specific functions implemented in software on the ARM CPU.

Other industry standard, peripheral interface controllers are supported, including UARTs with 16C550 device functionality. The UARTs support bit rates up to 115.2 kbps.

The I2C bus interface serves as master controllers. One 5 V-tolerant, 100/400KHz I2C bus is provided on the CX24138. GPIO ports can be used for interrupts, front panel control or for miscellaneous system handshake and control signals.

## 1.2.10 System I/O Bus Controller

The ISA-like I/O bus is provided to gluelessly attach to ROM/flash memory, hardware modem, and other peripherals. The ROM/flash memory data interface is up to 16-bits wide. Up to 22-bits of address bus is provided along with up to 4 chip selects, each of which allows access to 4M addressable memory locations.

## 1.3 CX24138 Pinout

The CX24138 family is housed in a 208-pin, MQFP package. The mechanical package drawing, pinout, pin descriptions, and I/O pad descriptions are provided in the following sections.

### 1.3.1 208 MQFP Package Drawing

Figures 3 and 4 are the 208-pin MQFP package drawing and pinout, respectively. The size parameters are listed in Table 1.

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**Figure 3. 208-Pin MQFP Package Drawing**

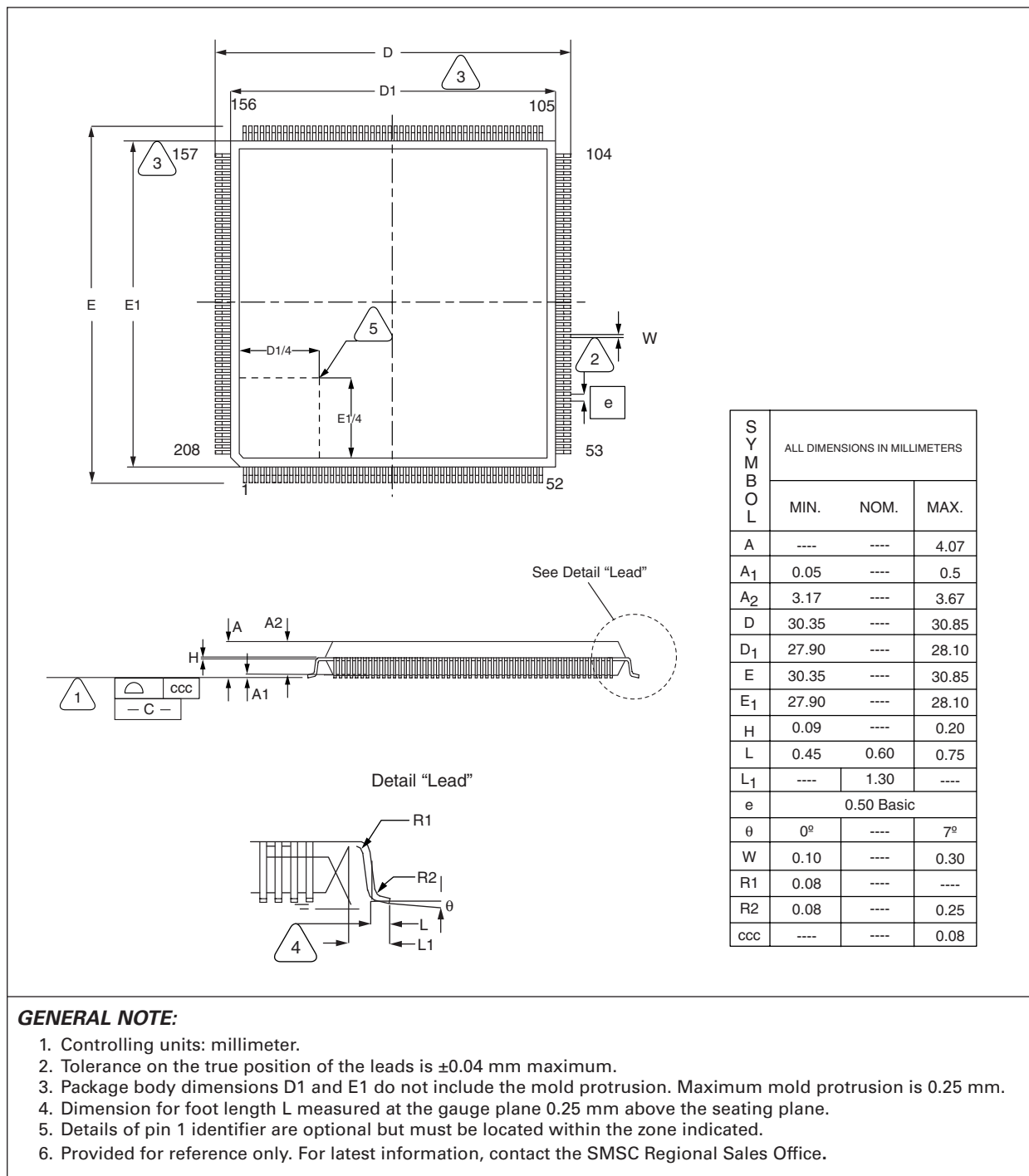
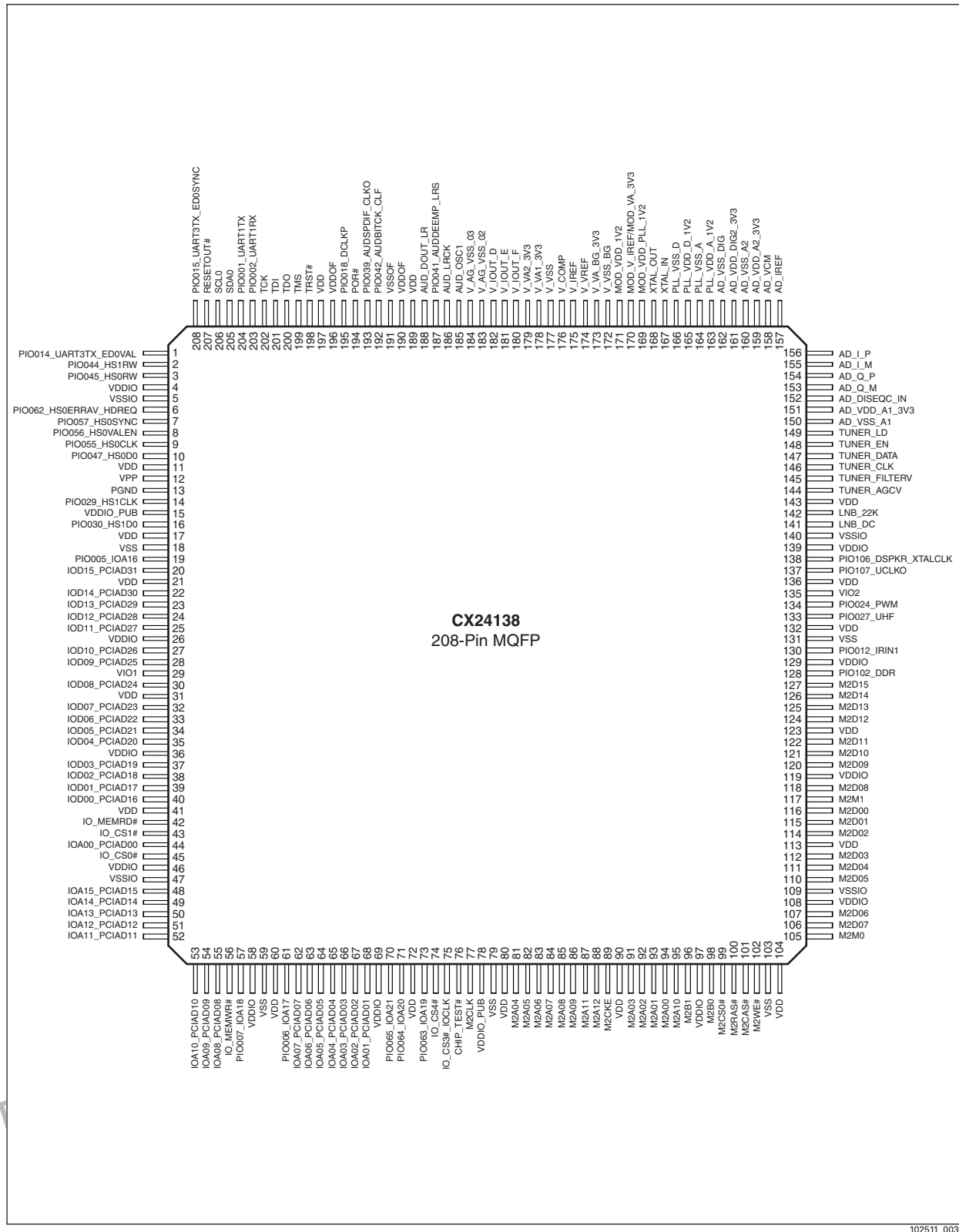


Figure 4. CX24138 Pinout



102511\_003

**Table 1. 208-Pin MQFP Size Parameters**

| Name                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Min   | Normal     | Max   | Remarks                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------|-------|------------------------|
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | -     | —          | 4.07  | Overall Package Height |
| A1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0.05  | —          | 0.5   | Standoff               |
| A2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 3.17  | —          | 3.67  | Body Thickness         |
| D                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 30.35 | —          | 30.85 | X Span                 |
| D1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 27.90 | —          | 28.10 | X Body Size            |
| E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 30.35 | —          | 30.85 | Y Span                 |
| E1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 27.90 | —          | 28.10 | Y Body Size            |
| H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0.09  | —          | 0.20  | Lead Frame Thickness   |
| L                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0.45  | 0.60       | 0.75  | Lead Foot Length       |
| L1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | -     | 1.30       | -     | Lead Length            |
| e                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |       | 0.50 Basic |       | Lead Pitch             |
| q                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0°    | —          | 7°    | Lead Foot Angle        |
| W                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0.10  | —          | 0.30  | Lead Width             |
| R1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0.08  | —          | -     | Lead Shoulder Radius   |
| R2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0.08  | —          | 0.25  | Lead Foot Radius       |
| ccc                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -     | —          | 0.08  | Coplanarity            |
| <b>GENERAL NOTE:</b><br>1. Controlling Units: millimeter.<br>2. Tolerance on the true position of the leads is $\pm 0.04$ mm maximum.<br>3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.<br>4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.<br>5. Details of pin 1 identifier are optional but must be located within the zone indicated.<br>6. This table is provided for reference only—contact SMSC Regional Sales Office for latest information. |       |            |       |                        |

## 1.3.2 CX24138 Pinlist

The pinlist for the CX24138 family is described in [Tables 2](#) and [3](#). CX24138 PIO pins power up as inputs and most of these pins contain an internal 330 k. pullup to 3.3 V. While most PIO pins provide internal pullup resistors, the internal pullups should not be used to pull up external devices on the printed circuit board. Nets that need to be pulled up or down should utilize an external 7.5 k. or smaller resistor. PIO pins that do not provide internal pullup resistors are denoted below. PIO pins can be configured as inputs, outputs, or sources of active high or low interrupt. Most inputs on the CX24138 provide hysteresis. The pinlist tables include a column that denotes the type of I/O pad used, such as pd\_pio or pd\_pio\_5v.

Use the following pin type definitions when reviewing [Tables 2](#) and [3](#). This list defines the suffixes that are used in the I/O Pad Type column of these two tables to ultimately describe the characteristics of the pad. The suffixes are the final set of letters after the final underscore. For example, the PIO106\_DSPKR\_XTALCLK pin lists an I/O Pad Type of pd\_pio\_5v\_sr. According to Table 2, “s” denotes a slow 2mA driver, while “r” represents a resistive pullup. The PIO106\_DSPKR\_XTALCLK pin is thus an I/O with 2mA source/sink capability and an internal resistive pullup.

| Pin Type<br>(I/O Pad Type Suffix) | Pin Type Definition                                                                   |
|-----------------------------------|---------------------------------------------------------------------------------------|
| r                                 | 330 k $\Omega$ internal resistive pullup                                              |
| s                                 | Slow speed (~5.8ns rise/5/7ns fall into 20pF load *), 2mA sink/source drive strength  |
| m                                 | Medium speed (~3.3ns rise/3.4ns fall into 20pF load*), 5mA sink/source drive strength |
| f                                 | Fast speed (~2.85ns rise/2.85ns fall into 20pF load*), 6mA sink/source drive strength |
| pho                               | High current PIO for directly driving LEDs, 12mA sink/source drive strength           |
| e                                 | Pseudo open drain (driver input is grounded and data controls output enable)          |
| od                                | Open drain                                                                            |
| pci                               | 3 V signaling PCI pad. This pin is not 5 V tolerant.                                  |
| 5v                                | 5V tolerant, clamped to VIO pin                                                       |

**GENERAL NOTE:** The rise/fall times represent approximate design targets, not actual characterized rise/fall data. Data is provided to give an idea of the rise/fall times that might be seen on a PCB design.

**Table 2. CX24138 Pinlist (1 of 11)**

| Pin Number                                                                                                                                                                                                                                                                                                                                                               | Pin Name    | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | I/O Pad Type  | Pin Direction |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|
| <b>TV Encoder – Pins for the Internal TV Encoder</b> <ul style="list-style-type: none"> <li>– Designs that use the internal TV encoder should connect pins as described in this pinlist.</li> <li>– Designs not using all 3 DAC outputs should leave unused DACs unconnected (not attached to load resistors), and unused DACs disabled via software control.</li> </ul> |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               |               |
| 182                                                                                                                                                                                                                                                                                                                                                                      | V_IOUT_D    | Baseband Video DAC output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Analog Signal |               |
| 181                                                                                                                                                                                                                                                                                                                                                                      | V_IOUT_E    | Baseband Video DAC output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Analog Signal |               |
| 180                                                                                                                                                                                                                                                                                                                                                                      | V_IOUT_F    | Baseband Video DAC output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Analog Signal |               |
| 175                                                                                                                                                                                                                                                                                                                                                                      | V_IREF      | Full Scale adjust control pin. External resistor connected between this pin and GND controls the full-scale DAC output current. Resistor value is $887\Omega \pm 1\%$ for high impedance DAC loads or $301\Omega \pm 1\%$ for low impedance DAC loads. See applications information for further details.                                                                                                                                                                                                                                                                     | Analog Signal |               |
| 176                                                                                                                                                                                                                                                                                                                                                                      | V_COMP      | Compensation pin. A 1.0uF ceramic capacitor in series with a $22\Omega \pm 5\%$ resistor must be used to decouple this pin to the V_VAx_3 V3 supply. The resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.                                                                                                                                                                                                                                                                                                      | Analog Signal |               |
| 174                                                                                                                                                                                                                                                                                                                                                                      | V_VREF      | Voltage reference pin. A 1.0uF capacitor must be used to decouple this pin to GND. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.                                                                                                                                                                                                                                                                                                                                                                                     | Analog Signal |               |
| 178                                                                                                                                                                                                                                                                                                                                                                      | V_VA1_3V3   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Analog Power  |               |
| 179                                                                                                                                                                                                                                                                                                                                                                      | V_VA2_3V3   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               |               |
|                                                                                                                                                                                                                                                                                                                                                                          |             | Video DAC power. All designs that utilize the internal VDACS must drive these pins through an external voltage drop resistor that is attached to a Nominal supply = 3.3 V $\pm 5\%$ . When operating with low impedance DAC load resistors, the external VDACS supply voltage drop resistor is $2.74\Omega \pm 1\%$ . When operating with high impedance DAC load resistors, the external VDACS supply voltage drop resistor is $13\Omega \pm 5\%$ . The voltage drop resistor values specified here should be used regardless of how many video DAC outputs are being used. |               |               |
| 172                                                                                                                                                                                                                                                                                                                                                                      | V_VSS_BG    | Video DAC Bandgap Ground. Tie to analog GND plane.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Analog Power  |               |
| 183                                                                                                                                                                                                                                                                                                                                                                      | V_AG_VSS_02 | Video DAC 3.3 V Gnd. Tie to analog GND plane                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Analog Power  |               |
| 184                                                                                                                                                                                                                                                                                                                                                                      | V_AG_VSS_03 | Video DAC 3.3 V Gnd. Tie to analog GND plane                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Analog Power  |               |
| 177                                                                                                                                                                                                                                                                                                                                                                      | V_VSS       | Video DAC ground tie for substrate bias. Tie to analog GND plane.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Analog Power  |               |
| 173                                                                                                                                                                                                                                                                                                                                                                      | V_VA_BG_3V3 | Video DAC Bandgap power. This pin ties to analog 3.3 V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Analog Power  |               |

**Table 2. CX24138 Pinlist (2 of 11)**

| Pin Number                                                                                                                                                                                                                                                                                                                                                                                   | Pin Name                  | Pin Description                                                                                                                                                                                                                                                     | I/O Pad Type  | Pin Direction |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|
| <b>RF Modulator – Pins for the RF Modulator Circuit</b> <ul style="list-style-type: none"> <li>MOD_VDD_PLL_1V2 and MOD_VDD_1V2 are tied to a common 1.25 V nominal supply rail and decoupled to ground with a single 0.1uF capacitor.</li> <li>MOD_VA_3V3 and MOD_V_IREF are tied together to a 3.3 V supply rail directly and decoupled to ground with a single 0.1uF capacitor.</li> </ul> |                           |                                                                                                                                                                                                                                                                     |               |               |
| 170                                                                                                                                                                                                                                                                                                                                                                                          | MOD_V_IREF/<br>MOD_VA_3V3 | Analog supply for RF mod. Nominal supply = 3.3 V $\pm$ 5%.                                                                                                                                                                                                          | Analog Power  |               |
| 169                                                                                                                                                                                                                                                                                                                                                                                          | MOD_VDD_PLL_1V2           | RF modulator PLL supply. Nominal supply = 1.25 V $\pm$ 5%.                                                                                                                                                                                                          | Analog Power  |               |
| 171                                                                                                                                                                                                                                                                                                                                                                                          | MOD_VDD_1V2               | RF modulator 1.25 V supply. Nominal supply = 1.25 V $\pm$ 5%.                                                                                                                                                                                                       | Analog Power  |               |
| <b>QPSK Demodulator - Pins for the Integrated QPSK Demodulator</b> <p>Designs that use the internal QPSK demodulator should connect pins as described in the pinlist section below and as shown in applications material.</p>                                                                                                                                                                |                           |                                                                                                                                                                                                                                                                     |               |               |
| 142                                                                                                                                                                                                                                                                                                                                                                                          | LNB_22K                   | LNB control signal.                                                                                                                                                                                                                                                 | pd_pio_f      | I/O           |
| 141                                                                                                                                                                                                                                                                                                                                                                                          | LNB_DC                    | Used to switch LNB polarity. Can be used asGPIO(1) if so programmed.                                                                                                                                                                                                | pd_pio_s      | I/O           |
| 152                                                                                                                                                                                                                                                                                                                                                                                          | AD_DISEQC_IN              | DiSEQ2.x input pin.                                                                                                                                                                                                                                                 |               |               |
| 157                                                                                                                                                                                                                                                                                                                                                                                          | AD_IREF                   | ADC Current Reference. External 30.9 k $\Omega$ $\pm$ 1% resistor connected between this pin and GND sets the reference current for the A/D converter. This pin should also be capacitively decoupled to GND using either a single 0.1uF or two 0.047uF capacitors. | Analog Signal |               |
| 158                                                                                                                                                                                                                                                                                                                                                                                          | AD_VCM                    | ADC common mode voltage reference. Capacitively decouple this pin to GND using a 0.01uF capacitor.                                                                                                                                                                  | Analog Signal |               |
| 154                                                                                                                                                                                                                                                                                                                                                                                          | AD_Q_P                    | ADC analog Input Ch1 +Q. When the CX24138 is used with the CX24108/CX24109 tuner, the Q_OUTP pin on the tuner should be left unconnected, and the AD_Q_P pin on the CX24138 should be tied to ground through an 0.01uF capacitor.                                   | Analog Signal |               |
| 153                                                                                                                                                                                                                                                                                                                                                                                          | AD_Q_M                    | ADC analog Input Ch1 -Q. The AD_Q_M pin is capacitively coupled to the CX24108/CX24109 Q_OUTN pin through a 1uF capacitor.                                                                                                                                          | Analog Signal |               |

**Table 2. CX24138 Pinlist (3 of 11)**

| Pin Number | Pin Name        | Pin Description                                                                                                                                                                                                                                      | I/O Pad Type  | Pin Direction |
|------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|
| 156        | AD_I_P          | ADC analog Input Ch1 +I. When the CX24138 is used with the CX24108/CX24109 tuner, the I_OUTP pin on the tuner should be left unconnected, and the AD_I_P pin on the CX24138 should be tied to ground through an 0.01uF capacitor.                    | Analog Signal |               |
| 155        | AD_I_M          | ADC analog Input Ch1 -I. The AD_I_M pin is capacitively coupled to the CX24108/CX24109 I_OUTN pin through a 1uF capacitor.                                                                                                                           | Analog Signal |               |
| 145        | TUNER_FILTERV   | Output of sigma-delta 1-bit DAC to control the filter in the tuner.                                                                                                                                                                                  | pd_pio_m      | 0             |
| 144        | TUNER_AGCv      | Output of sigma-delta 1-bit DAC to control the gain level of the analog signal in the tuner.                                                                                                                                                         | pd_pio_m      | 0             |
| 149        | TUNER_LD        | Used to get the tuner lock status.                                                                                                                                                                                                                   | pd_pio_sr     | 1             |
| 148        | TUNER_EN        | Used to communicate with the tuner. In Rosie-Mode, needs to be '1' before any transfer of data and set back to '0' to latch the data in the tuner. Can be used in bit-by-bit transfer or byte (burst) transfer. In Viper-Mode, it is not being used. | pd_pio_s      | 0             |
| 147        | TUNER_DATA      | Data signal to the tuner. This is common for both tuners. The signal that differs between them is the TUNER_EN_x. In Viper-Mode, it will transfer data either direction.                                                                             | pd_pio_sr     | 0             |
| 146        | TUNER_CLK       | Clock signal to the tuner. This is the data clock and it is common for both tuners. The signal that differs between them is: TUNER_EN_x (see above).                                                                                                 | pd_pio_s      | 0             |
| 151        | AD_VDD_A1_3V3   | Demodulator ADC Power supplies. Nominal supply = 3.3 V $\pm$ 5%.                                                                                                                                                                                     | Analog Power  |               |
| 159        | AD_VDD_A2_3V3   |                                                                                                                                                                                                                                                      | Analog Power  |               |
| 161        | AD_VDD_DIG2_3V3 | Demodulator ADC Power supplies. Nominal supply = 3.3 V $\pm$ 5%.                                                                                                                                                                                     | Analog Power  |               |
| 150        | AD_VSS_A1       | Demodulator ADC Power supplies. Tie to analog GND plane                                                                                                                                                                                              | Analog Power  |               |
| 160        | AD_VSS_A2       |                                                                                                                                                                                                                                                      | Analog Power  |               |
| 162        | AD_VSS_DIG      | Demodulator ADC Power supplies. This pin supplies ground connection to the Demodulator ADC. Tie to analog GND plane                                                                                                                                  | Analog Power  |               |

**Table 2. CX24138 Pinlist (4 of 11)**

| Pin Number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Pin Name      | Pin Description                                                                                                                                                                                                                                                                                                                                                                                 | I/O Pad Type  | Pin Direction |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|
| 163                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PLL_VDD_A_1V2 | Demodulator PLL Power Supplies. Nominal supply = 1.25 V ± 5%.                                                                                                                                                                                                                                                                                                                                   | Analog Power  |               |
| 165                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PLL_VDD_D_1V2 |                                                                                                                                                                                                                                                                                                                                                                                                 | Analog Power  |               |
| 164                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PLL_VSS_A     | Demodulator PLL Power Supplies. Tie to analog GND plane.                                                                                                                                                                                                                                                                                                                                        | Analog Power  |               |
| 166                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PLL_VSS_D     |                                                                                                                                                                                                                                                                                                                                                                                                 | Analog Power  |               |
| Crystal oscillator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |               |                                                                                                                                                                                                                                                                                                                                                                                                 |               |               |
| 167                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | XTAL_IN       | Crystal oscillator input. XTl can be driven by an external crystal oscillator, or a crystal can be connected between XTALI and XTALO to utilize the on-board crystal oscillator circuit.Designs should utilize a 10.111MHz crystal, or accept a 10.111MHz clock from the CX24109 tuner if the design is so equipped.See applications information for details on crystal circuit configurations. | Analog Signal |               |
| 168                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | XTAL_OUT      | Crystal amplifier output                                                                                                                                                                                                                                                                                                                                                                        | Analog Signal |               |
| JTAG Debugger/Boundary Scan Interface                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                                                                                                                                                                                                                                                                                                                                                                                                 |               |               |
| A JTAG Debugger must be attached to these pins during the early stages of PCB design for software development/board debug. Pins should be connected to the JTAG Debugger unit with pullup/pulldown resistors as specified in the pinlist below. and illustrated in the application materials for the CX24138 device.Mature designs for which no software development or board debug is required, and designs which must leave JTAG pins tied off or unconnected per conditional access provider mandate, should treat unused pins as specified in the pinlist below. |               |                                                                                                                                                                                                                                                                                                                                                                                                 |               |               |
| 202                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | TCK           | JTAG test clock. Used to synchronize all JTAG test structures. Pin should be pulled low when JTAG operations are not being performed. TCK operates on both the JTAG tap controller and the ARM tap controller.                                                                                                                                                                                  | pd_pio        | I             |
| 201                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | TDI           | JTAG test data input. Loads instructions into the TAP controller or loads test vector data for boundary-scan operation. Pin is pulled high when JTAG operations are not being performed.                                                                                                                                                                                                        | pd_pio_r      | I             |
| 200                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | TDO           | JTAG test data output                                                                                                                                                                                                                                                                                                                                                                           | pd_pio_m      | O             |
| 199                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | TMS           | JTAG test mode select for the boundary scan tap controller. Transitions on this pin drive the JTAG state machine through its sequences. Pin should be pulled high when JTAG operations are not being performed.                                                                                                                                                                                 | pd_pio_r      | I             |
| 198                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | TRST#         | Test Reset / Mode Enable. Initializes the JTAG tap controller. This pin should be driven by the external power on reset controller circuit.                                                                                                                                                                                                                                                     | pd_pio_r      | I             |
| 76                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | CHIP_TEST#    | Pin used for automated testing purposes only. Customer designs should leave this pin floating.                                                                                                                                                                                                                                                                                                  | pd_pio_r      | I             |

**Table 2. CX24138 Pinlist (5 of 11)**

| Pin Number                                                                                                                                                                                                         | Pin Name | Pin Description                                                                                                                                                                                                                                                                                                                                                                    | I/O Pad Type | Pin Direction |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| <b>MPEG Subsystem SDRAM Interface</b><br>Series termination of SDRAM data signals and the SDRAM clock signal are recommended. It is uncommon for other SDRAM interface signals to require any form of termination. |          |                                                                                                                                                                                                                                                                                                                                                                                    |              |               |
| 116                                                                                                                                                                                                                | M2D00    | Bidirectional three-state SDRAM memory data. The memory interface is 16-bit wide. Bit 15 is most significant.<br><br>It is recommended that SDRAM data signals be series terminated to slow down the edge rates of the SDRAM during SDRAM read cycles. Very fast edge transitions on the SDRAM device can cause the power supplies to drop by 400 mV to 800 mV during read cycles. | pd_pio_fr    | I/O           |
| 115                                                                                                                                                                                                                | M2D01    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 114                                                                                                                                                                                                                | M2D02    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 112                                                                                                                                                                                                                | M2D03    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 111                                                                                                                                                                                                                | M2D04    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 110                                                                                                                                                                                                                | M2D05    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 107                                                                                                                                                                                                                | M2D06    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 106                                                                                                                                                                                                                | M2D07    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 118                                                                                                                                                                                                                | M2D08    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 120                                                                                                                                                                                                                | M2D09    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 121                                                                                                                                                                                                                | M2D10    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 122                                                                                                                                                                                                                | M2D11    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 124                                                                                                                                                                                                                | M2D12    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 125                                                                                                                                                                                                                | M2D13    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 126                                                                                                                                                                                                                | M2D14    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| 127                                                                                                                                                                                                                | M2D15    |                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |

**Table 2. CX24138 Pinlist (6 of 11)**

| Pin Number | Pin Name | Pin Description                                                                                           | I/O Pad Type | Pin Direction |
|------------|----------|-----------------------------------------------------------------------------------------------------------|--------------|---------------|
| 94         | M2A00    | Row/Column address lines to SDRAM.                                                                        | pd_pio_f     | 0             |
| 93         | M2A01    |                                                                                                           | pd_pio_f     | 0             |
| 92         | M2A02    |                                                                                                           | pd_pio_f     | 0             |
| 91         | M2A03    |                                                                                                           | pd_pio_f     | 0             |
| 81         | M2A04    |                                                                                                           | pd_pio_f     | 0             |
| 82         | M2A05    |                                                                                                           | pd_pio_f     | 0             |
| 83         | M2A06    |                                                                                                           | pd_pio_f     | 0             |
| 84         | M2A07    |                                                                                                           | pd_pio_f     | 0             |
| 85         | M2A08    |                                                                                                           | pd_pio_f     | 0             |
| 86         | M2A09    |                                                                                                           | pd_pio_f     | 0             |
| 95         | M2A10    |                                                                                                           | pd_pio_f     | 0             |
| 87         | M2A11    |                                                                                                           | pd_pio_f     | 0             |
| 88         | M2A12    |                                                                                                           | pd_pio_f     | 0             |
| 105        | M2M0     | SDRAM data input/output mask.                                                                             | pd_pio_f     | 0             |
| 117        | M2M1     |                                                                                                           | pd_pio_f     | 0             |
| 89         | M2CKE    | SDRAM clock enable.                                                                                       | pd_pio_f     | 0             |
| 77         | M2CLK    | SDRAM memory clock output. This pin should be series terminated to improve signal integrity at the SDRAM. | pd_ckio      | 0             |
| 98         | M2B0     | Lower bank address select.                                                                                | pd_pio_f     | 0             |
| 96         | M2B1     | Upper bank address select.                                                                                | pd_pio_f     | 0             |
| 100        | M2RAS#   | SDRAM row address strobe.                                                                                 | pd_pio_f     | 0             |
| 102        | M2WE#    | SDRAM write enable.                                                                                       | pd_pio_f     | 0             |
| 99         | M2CS0#   | SDRAM chip select.                                                                                        | pd_pio_f     | 0             |
| 101        | M2CAS#   | SDRAM column address strobe command.                                                                      | pd_pio_f     | 0             |

**Table 2. CX24138 Pinlist (7 of 11)**

| Pin Number                                                                                                                                   | Pin Name              | Pin Description                                                                                                                                                                                                                                                             | I/O Pad Type  | Pin Direction |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|
| Pins that Provide Only PIO Functionality                                                                                                     |                       |                                                                                                                                                                                                                                                                             |               |               |
| 195                                                                                                                                          | PIO018_DCLKP          | Pin comes up as a PIO input. These pins can be independently configured for active high or low, edge or level triggered interrupt, or configured as outputs.<br><br>Note that PIO102 has 12mA source/sink capability for driving an LED without external drive transistors. | pd_ssd_pwrclk | I/O           |
| 128                                                                                                                                          | PIO102_DDR            |                                                                                                                                                                                                                                                                             | pd_pho_r      | I/O           |
| 14                                                                                                                                           | PIO029_HS1CLK         |                                                                                                                                                                                                                                                                             | pd_pio_fr     | I/O           |
| 16                                                                                                                                           | PIO030_HS1D0          |                                                                                                                                                                                                                                                                             | pd_pio_fr     | I/O           |
| 2                                                                                                                                            | PIO044_HS1RW          |                                                                                                                                                                                                                                                                             | pd_pio_5v_fr  | I/O           |
| 3                                                                                                                                            | PIO045_HS0RW          |                                                                                                                                                                                                                                                                             | pd_pio_5v_fr  | I/O           |
| Serial High-Speed Dataport 0 - These pins come up as PIO pins and can be reconfigured by firmware to serve as a serial high-speed data port. |                       |                                                                                                                                                                                                                                                                             |               |               |
| 6                                                                                                                                            | PIO062_HS0ERRAV_HDREQ | Pin comes up as a PIO input pin and can be configured by firmware as a transport stream error indicator.                                                                                                                                                                    | pd_pio_5v_fr  | I/O           |
| 7                                                                                                                                            | PIO057_HS0SYNC        | Pin comes up as a PIO input pin and can be configured by firmware as a transport stream sync indicator.                                                                                                                                                                     | pd_pio_5v_fr  | I/O           |
| 8                                                                                                                                            | PIO056_HS0VALEN       | Pin comes up as a PIO input pin and can be configured by firmware as a transport stream valid indicator.                                                                                                                                                                    | pd_pio_5v_fr  | I/O           |
| 9                                                                                                                                            | PIO055_HS0CLK         | Pin comes up as a PIO input pin and can be configured by firmware as a transport stream clock signal.                                                                                                                                                                       | pd_pio_5v_fr  | I/O           |
| 10                                                                                                                                           | PIO047_HS0D0          | Pin comes up as a PIO input pin and can be configured by firmware as a serial transport stream data I/O pin.                                                                                                                                                                | pd_pio_5v_fr  | I/O           |
| Digital Audio I/O                                                                                                                            |                       |                                                                                                                                                                                                                                                                             |               |               |
| 188                                                                                                                                          | AUD_DOUT_LR           | Attenuated PCM audio data output. In 6-channel output test mode, AUD_DOUT_LR will output left/right data. Also serves as a configuration input pin.                                                                                                                         | pd_pio_sr     | I/O           |
| 186                                                                                                                                          | AUD_LRCK              | Audio sample rate clock output. Also serves as a configuration input pin                                                                                                                                                                                                    | pd_pio_sr     | I/O           |
| 185                                                                                                                                          | AUD_OSC1              | OSC1 Oversampled clock output with selectable frequencies of 512 x Fs, 256 x Fs, 128 x Fs, 64 x Fs (where Fs is the sample frequency).Also serves as a configuration input pin.                                                                                             | pd_pio_sr     | I/O           |

**Table 2. CX24138 Pinlist (8 of 11)**

| Pin Number                                                                                                                                                               | Pin Name                | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                  | I/O Pad Type | Pin Direction |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 193                                                                                                                                                                      | PIO039_AUDSPDIF_CLKO    | Pin comes up as PIO input pin and can be configured by firmware as the AES/EBU digital audio output. Attaches to electrical or fiber-optic driver circuit. This pin can also be programmed to output a clock signal derived from the crystal circuit any of the five internal PLLs or the crystal input. When used as a clock or SPDIF output, this pin should usually be series terminated to improve signal integrity at the receiving device. | pd_pio_5v_fr | I/O           |
| 187                                                                                                                                                                      | PIO041_AUDDEEMP_LRS     | Pin comes up as PIO input pin and can be configured as the audio de-emphasis control output. Used to indicate the type of deemphasis used in the MPEG bit stream. The type of de-emphasis in use is software configurable. Choices include: no deemphasis, 50/15 ms, or CCITT J.17. In 6-channel output test mode, AUD_DEEMP_LRS will output left/right surround data.                                                                           | pd_pio_5v_sr | I/O           |
| 192                                                                                                                                                                      | PIO042_AUDBITCK_CLF     | Pin comes up as PIO input pin and can be configured by firmware as the audio bit rate clock output. In 6-channel output test mode, this pin will output center/low frequency output data.                                                                                                                                                                                                                                                        | pd_pio_5v_sr | I/O           |
| <b>Serial Communication</b><br>Includes UARTs, Infrared I/O, I2C.<br><b>NOTE:</b> UART1 is accessible via the CX24138 DMA engine. UART3 does not include DMA capability. |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |              |               |
| 204                                                                                                                                                                      | PIO001_UART1TX          | Pin comes up as PIO input pin and can be configured by firmware to transmit data from UART1.                                                                                                                                                                                                                                                                                                                                                     | pd_pio_5v_sr | I/O           |
| 203                                                                                                                                                                      | PIO002_UART1RX          | Pin comes up as PIO input pin and can be configured by firmware to accept data for UART1.                                                                                                                                                                                                                                                                                                                                                        | pd_pio_5v_sr | I/O           |
| 1                                                                                                                                                                        | PIO014_UART3TX_ED0VAL   | Pin comes up as PIO input pin and can be configured by firmware to transmit data from UART3.                                                                                                                                                                                                                                                                                                                                                     | pd_pio_5v_fr | I/O           |
| 208                                                                                                                                                                      | PIO015_UART3TX_ED0SY NC | Pin comes up as PIO input pin and can be configured by firmware to accept data for UART3.                                                                                                                                                                                                                                                                                                                                                        | pd_pio_5v_fr | I/O           |
| 130                                                                                                                                                                      | PIO012_IRIN1            | Pin comes up as PIO input pin and can be configured by firmware as the input signal from IR photo detector or receiver. This input accepts either modulated or unmodulated IR data.                                                                                                                                                                                                                                                              | pd_pio_5v_sr | I/O           |
| 133                                                                                                                                                                      | PIO027_UHF              | Pin comes up as PIO input pin and can be configured by firmware to measure TTL pulse width from devices such as IR or UHF remote controls. This input accepts only demodulated data.                                                                                                                                                                                                                                                             | pd_pio_5v_sr | I/O           |
| 206                                                                                                                                                                      | SCL0                    | IIC Bus 0 clock. This open drain style output driver requires a pullup to 3.3 V or 5 V for proper operation.                                                                                                                                                                                                                                                                                                                                     | pd_i2c_5v    | I/O           |

**Table 2. CX24138 Pinlist (9 of 11)**

| Pin Number                                                                  | Pin Name             | Pin Description                                                                                                                                                                                                                                                                     | I/O Pad Type | Pin Direction |
|-----------------------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 205                                                                         | SDA0                 | IIC Bus 0 data. This open drain style output driver requires a pullup to 3.3 V or 5 V for proper operation.                                                                                                                                                                         | pd_i2c_5v    | I/O           |
| <b>Miscellaneous Signals: Resets, Pulse Width Modulation, Clock Outputs</b> |                      |                                                                                                                                                                                                                                                                                     |              |               |
| 207                                                                         | RESETOUT#            | External reset output for resetting flash ROM and other devices in the system. The default delay between RESETOUT# deassertion and the first ROM read cycle is approximately 4.7uS.                                                                                                 | pd_pio_s     | 0             |
| 194                                                                         | POR#                 | Power-on reset input. Tie to an external power on reset controller. POR# must be asserted for at least 50uS.                                                                                                                                                                        | pd_pio_sr    | I             |
| 134                                                                         | PIO024_PWM           | Pin comes up as a PIO input and can be configured by firmware as a pulse width modulated output. Note that this PIO has 12mA source/sink capability for driving LEDs without external drive transistors.                                                                            | pd_pho_r     | I/O           |
| 138                                                                         | PIO106_DSPKR_XTALCLK | Pin comes up as PIO input pin and can output a buffered version of the clock input to the XTAL_IN pin. When used as a clock output, this pin should usually be series terminated to improve signal integrity at the receiving device.                                               | pd_pio_5v_fr | I/O           |
| 137                                                                         | PIO107_UCLKO         | Pin comes up as PIO input pin and can be programmed to output a clock signal derived from any of the five internal system PLLs or the crystal input. When used as a clock output, this pin should usually be series terminated to improve signal integrity at the receiving device. | pd_pio_5v_fr | I/O           |
| <b>I/O Bus Control Signals</b>                                              |                      |                                                                                                                                                                                                                                                                                     |              |               |
| 56                                                                          | IO_MEMWR#            | IO_MEMWR# output serves as the I/O bus memory write strobe and should be attached to FLASH ROM devices.                                                                                                                                                                             | pd_pio_f     | 0             |
| 42                                                                          | IO_MEMRD#            | IO_MEMRD# output serves as the I/O bus memory read strobe and should be attached to ROM, EPROM, and FLASH ROM devices.                                                                                                                                                              | pd_pio_f     | 0             |

**Table 2. CX24138 Pinlist (10 of 11)**

| Pin Number                                                                                                                                                                                                                                                                                                                      | Pin Name      | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | I/O Pad Type | Pin Direction |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 45                                                                                                                                                                                                                                                                                                                              | IO_CS0#       | General purpose I/O bus chip selects. In addition to serving as chip select outputs, these pins also serve as configuration register inputs. The status of these pins is latched into the chip at reset time and provide a means for hardware and software initialization. These pins are internally pulled up, but the pullup cannot be used to drive devices external to the CX24138. A 7.5 k $\Omega$ pullup or pulldown can be used to override the internal pullup and drive external devices on the net. The IO_CS3#_IOCLK pin can be reprogrammed to serve as a synchronous clock for the I/O bus interface instead of a chip select, thus enabling the I/O bus to be used as either a synchronous or asynchronous interface. Flash ROMs attached to IO_CS0 should be of the bottom boot block variety. | pd_pio_fr    | I/O           |
| 75                                                                                                                                                                                                                                                                                                                              | IO_CS3#_IOCLK |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | pd_pio_fr    | I/O           |
|                                                                                                                                                                                                                                                                                                                                 |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |              |               |
| 43                                                                                                                                                                                                                                                                                                                              | IO_CS1#       | Must be pulled up via a 7.5 k $\Omega$ pullup resistor to configure the CX24138 to operate in standard I/O mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | pd_pio_fr    | I/O           |
| 74                                                                                                                                                                                                                                                                                                                              | IO_CS4#       | Must be pulled down via a 7.5 k $\Omega$ pulldown resistor to configure the CX24138 to operate with 16-bit SDRAM interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | pd_pio_fr    | I/O           |
| <b>Digital Power</b><br>The CX24138 does not require that supply rails be sequenced in a particular order. Power supply rails can be brought up in any order without damaging the device; however, if the VDDIO rail is brought up first, the state of I/O pins will be indeterminate until the VDD rail reaches nominal value. |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |              |               |
| 13                                                                                                                                                                                                                                                                                                                              | PGND          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |              |               |
| 11,17,21,<br>31,41,60,<br>72,80,90,<br>104,113,<br>123,132,<br>136,143,<br>189,197                                                                                                                                                                                                                                              | VDD           | 1.25 V $\pm$ 5% Core Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Power Supply |               |
| 4,26,36,4<br>6,58,69,9<br>7,108,11<br>9,129,13<br>9                                                                                                                                                                                                                                                                             | VDDIO         | 3.3 V $\pm$ 5% I/O Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Power Supply |               |
| 15, 78                                                                                                                                                                                                                                                                                                                          | VDDIO_PUB     | Special I/O power pad that provides pull-up disable functionality to all of the I/O pads. Tied to 3.3 V like all the other VDDIO pads.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Power Supply |               |
| 29                                                                                                                                                                                                                                                                                                                              | VI01          | Reference voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Power Supply |               |
| 135                                                                                                                                                                                                                                                                                                                             | VI02          | ESD protection supply pin - Tie to 5 V $\pm$ 5% supply if 5 V I/O is present; otherwise tie to 3.3 V $\pm$ 5% supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Power Supply |               |

**Table 2. CX24138 Pinlist (11 of 11)**

| Pin Number        | Pin Name | Pin Description                                                                                                                                            | I/O Pad Type | Pin Direction |
|-------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 190, 196          | VDDOF    | Special power pads that provide power to both the internal fuse array (hence the notation 'f' for fuse). Tie it to the same 3.3 V rail that ties to vddio. | Power Supply |               |
| 12                | VPP      | System pll power, tied to the 1.25 V $\pm$ 5% core supply                                                                                                  | Power Supply |               |
| 18,59,79, 103,131 | VSS      | 1.25 V chip power supply ground                                                                                                                            | Power Supply |               |
| 5,47,109, 140     | VSSIO    | 3.3 V chip power supply ground                                                                                                                             | Power Supply |               |
| 191               | VSSOF    | Special power pads that provide power to both the internal fuse array (hence the notation 'f' for fuse). Tie it to the same 3.3 V rail that ties to vddio. | Power Supply |               |

**Table 3. CX24138 I/O Mode Pin Table**

| Pin Number                 | Pin Name     | Pin Description                                                                                                                                                         | I/O Pad Type | Pin Direction |
|----------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 19                         | PIO005_IOA16 | Pins come up as PIO input pin with an internal 330 k pullup. All PIO pins can be configured as inputs, outputs, or sources of active high or low interrupt to the chip. | pd_pio_fr    | I/O           |
| 61                         | PIO006_IOA17 |                                                                                                                                                                         | pd_pio_fr    | I/O           |
| 57                         | PIO007_IOA18 |                                                                                                                                                                         | pd_pio_fr    | I/O           |
| 73                         | PIO063_IOA19 |                                                                                                                                                                         | pd_pio_fr    | I/O           |
| 71                         | PIO064_IOA20 |                                                                                                                                                                         | pd_pio_fr    | I/O           |
| 70                         | PIO065_IOA21 |                                                                                                                                                                         | pd_pio_fr    | I/O           |
| I/O Data and Address Buses |              |                                                                                                                                                                         |              |               |

**Table 3. CX24138 I/O Mode Pin Table**

| Pin Number | Pin Name      | Pin Description                                                                                                   | I/O Pad Type | Pin Direction |
|------------|---------------|-------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 40         | IOD00_PCIAD16 | I/O Data Bus for the CX24138. IOD[15:0] is used to attach parallel flash ROM devices. Bit 0 is least significant. | pd_pci       | I/O           |
| 39         | IOD01_PCIAD17 |                                                                                                                   | pd_pci       | I/O           |
| 38         | IOD02_PCIAD18 |                                                                                                                   | pd_pci       | I/O           |
| 37         | IOD03_PCIAD19 |                                                                                                                   | pd_pci       | I/O           |
| 35         | IOD04_PCIAD20 |                                                                                                                   | pd_pci       | I/O           |
| 34         | IOD05_PCIAD21 |                                                                                                                   | pd_pci       | I/O           |
| 33         | IOD06_PCIAD22 |                                                                                                                   | pd_pci       | I/O           |
| 32         | IOD07_PCIAD23 |                                                                                                                   | pd_pci       | I/O           |
| 30         | IOD08_PCIAD24 |                                                                                                                   | pd_pci       | I/O           |
| 28         | IOD09_PCIAD25 |                                                                                                                   | pd_pci       | I/O           |
| 27         | IOD10_PCIAD26 |                                                                                                                   | pd_pci       | I/O           |
| 25         | IOD11_PCIAD27 |                                                                                                                   | pd_pci       | I/O           |
| 24         | IOD12_PCIAD28 |                                                                                                                   | pd_pci       | I/O           |
| 23         | IOD13_PCIAD29 |                                                                                                                   | pd_pci       | I/O           |
| 22         | IOD14_PCIAD30 |                                                                                                                   | pd_pci       | I/O           |
| 20         | IOD15_PCIAD31 |                                                                                                                   | pd_pci       | I/O           |

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**Table 3. CX24138 I/O Mode Pin Table**

| Pin Number | Pin Name      | Pin Description                                                                                                                                                                                                                                                                                                                                     | I/O Pad Type | Pin Direction |
|------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|
| 44         | IOA00_PCIAD00 | I/O Address bus for the CX24138. The default configuration for the CX24138 allows 19 bits of I/O address space for access to 1Mbytes of ROM. Up to 22 bits of ROM address space (IOA[21:0]) can be made available by loading the configuration inputs associated with pins PIO006_IOA17 and PIO005_IOA16 at reset time. Bit 0 is least significant. | pd_pci       | I/O           |
| 68         | IOA01_PCIAD01 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 67         | IOA02_PCIAD02 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 66         | IOA03_PCIAD03 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 65         | IOA04_PCIAD04 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 64         | IOA05_PCIAD05 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 63         | IOA06_PCIAD06 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 62         | IOA07_PCIAD07 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 55         | IOA08_PCIAD08 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 54         | IOA09_PCIAD09 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 53         | IOA10_PCIAD10 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 52         | IOA11_PCIAD11 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 51         | IOA12_PCIAD12 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 50         | IOA13_PCIAD13 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 49         | IOA14_PCIAD14 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |
| 48         | IOA15_PCIAD15 |                                                                                                                                                                                                                                                                                                                                                     | pd_pci       | I/O           |

## 1.4 Configuration Pin Use

The CX24138 contains a configuration register that provides a mechanism to load information about the PCB configuration. The configuration register loads by sampling various pins on the chip during reset. 7.5 k $\Omega$  or smaller pull-up/pull-down resistors attached to these pins drive the pins high or low, thus loading a 1 or 0 into each corresponding bit within the configuration register. After reset, these pins resume their normal function.

Configuration input pins are pulled up with a 330 k $\Omega$  resistor inside the CX24138. While this resistor is sufficient to pull-up an otherwise undriven net, the internal pullup cannot be used to drive other devices on the board. If external devices need to be pulled up, or pulled-down, then a 7.5 k $\Omega$  or smaller pull-up or pull-down should be installed on the board. The CX24138 pin list should be consulted to see which pins do and do not include internal pullup resistors.

The use of 7.5 k $\Omega$  or smaller pulldown resistors to load the configuration register provides some limitations on the type of external hardware that can be attached to the pins used as configuration inputs. Only high impedance CMOS devices can be attached to these pins. Use of standard TTL or LS-TTL devices on these pins will cause the configuration register to be loaded with incorrect values.

See the “System Registers” chapter of the CX2414X specification for information on the “Configuration Register”.

## 1.4.1 CX24138 Configuration Register—Hardware Initialization

CX24138 uses configuration resistors to either directly affect logic inside the CX24138 or simply to load a value into a register for subsequent interrogation by software. Pins used to directly affect the operation of logic inside the CX24138 and provide immediate hardware initialization include the AUD\_OSC1, IO\_CS0#, IO\_CS3#, PIO006\_IOA17, and PIO005\_IOA16 pins. These pins are listed in [Tables 4](#) and [5](#) along with the description of logic functions they can affect.

### 1.4.1.1 Hardware Initialization Bits Not Used on Production Designs

The configuration register input AUD\_OSC1 in the CX24138, described in [Table 4](#), is intended for chip test and debug purposes and should not be used in production designs.

#### PLL Bypass Enable

The AUD\_OSC1 pin can be used to place the CX24138 into PLL bypass mode. When this pin is pulled low, the CX24138 derives clock inputs from several different pins within the CX24138 pinout. PLL bypass mode would not be used during normal operation of the CX24138, and is typically used only during ATE testing. Customer applications would not utilize PLL bypass mode, and would therefore rely on the internal pull up to pull the AUD\_OSC1 pin high during reset.

**Table 4. Unused Hardware Configuration Bits**

| Function        | Config Bit # | Signal Name | Bit Definition                                  | Used In Production CX24138 Designs?                                        |
|-----------------|--------------|-------------|-------------------------------------------------|----------------------------------------------------------------------------|
| PLL Bypass Mode | 31           | AUD_OSC1    | 0 = Bypass Internal PLL<br>1 = Use Internal PLL | This bit is not used in production designs and should always be left high. |

### 1.4.1.2 Hardware Initialization Bits Required for Customer Designs

The remaining configuration register bits that directly affect hardware initialization within the CX24138 are initialized by the power on reset state of IO\_CS0#, IO\_CS3#, PIO006\_IOA17, and PIO005\_IOA16. Pull down resistors should typically be provided for these pins to affect the operation of the CX24138 as described below. [Table 5](#) summarizes the hardware initialization configuration bits used on customer designs.

#### I/O Address Bus Width Select

The PIO006\_IOA17, and PIO005\_IOA16 pins are used to inform the CX24138 how wide the I/O address bus should be at boot time when the device is in standard I/O bus mode. In standard I/O bus mode, the CX24138 defaults to a 19-bit wide address bus allowing access to 1Mbytes of ROM (using 16-bit wide ROM devices). The address bus can be extended up to a 22-bit wide bus using the Address Bus Width configuration pins, but only at the expense of consuming PIO pins. Pins multiplexed with the I/O address bus include the following pins: PIO065\_IOA21, PIO064\_IOA20, and PIO063\_IOA19.

### Boot ROM Width Select

The IO\_CS0# pin informs the CX24138 the width of the boot ROM being used. The CX24138 ROM interface logic must know what width ROMs are being used prior to fetching the first instruction from ROM. Install a 7.5 k $\Omega$  pulldown resistor on IO\_CS0# if 8-bit wide ROMs are in use. Leave IO\_CS0# floating or pulled up with a 7.5 k $\Omega$  resistor if 16-bit wide ROMs are in use.

### High vs. Low Frequency Crystal In Use

The IO\_CS3# pin informs the CX24138 whether a high frequency or a low frequency crystal is in use. Leave IO\_CS3# floating or pulled up with a 7.5 k $\Omega$  resistor. When this configuration bit is pulled high or left floating, an internal divider is bypassed and the system PLLs are supplied with the base crystal frequency. When this configuration bit is pulled low an internal divide-by-4 circuit pre-divides the clock to the system PLLs so that the system PLLs always see approximately the same frequency range, regardless of what speed crystal is attached.

**Table 5. Required Hardware Configuration Bits**

| Function                                   | Config Bit # | Signal Name                  | Bit Definition                                                           | Used In Production Designs? |
|--------------------------------------------|--------------|------------------------------|--------------------------------------------------------------------------|-----------------------------|
| I/O Address Bus Width in Standard I/O Mode | 12<br>11     | PI0006_IOA17<br>PI0005_IOA16 | 11 = 22 bit bus<br>10 = 21 bit bus<br>01 = 20 bit bus<br>00 = 19 bit bus | Yes                         |
| ROM Width                                  | 27           | IO_CS0#                      | 0 = 8 Bit ROM<br>1 = 16 Bit ROM                                          | Yes                         |
| High- Versus Low-Frequency Crystal in Use  | 03           | IO_CS3#                      | 0 = high frequency crystal in use<br>1 = low frequency crystal in use    | Yes                         |

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# 2

## Register Index

Table 6 lists the CX24138 memory-mapped registers. The actual register names used in coding contain a prefix and suffix, which are not shown with each name. The prefix and suffix are listed in the header line of each register category. The CX24138 registers are the same as those described in *CX2414X Interactive TVDecoder IC Manual*, except that the registers listed with an asterisk \* in the column to the left of the "Register Name" column have different definitions from the CX2414X definitions. For more information about the listed registers, see the page listed in the "Refer to CX2414X Document 102210B" column. The differences between the CX2414X and CX24138 are listed in Chapter 3.

**Table 6. CX24138 Register Index (1 of 20)**

| *                                                                | Register Name    | Address   | Description                                                                                                | Refer to CX2414X Document 102210B |
|------------------------------------------------------------------|------------------|-----------|------------------------------------------------------------------------------------------------------------|-----------------------------------|
| <b>System Controller (300000xxh) - prefix: RST_ suffix: _REG</b> |                  |           |                                                                                                            |                                   |
|                                                                  | STATUS           | 30000000h | Contains the source of a reset.                                                                            | page 5-7                          |
|                                                                  | SUSPEND          | 30000004h | Temporarily stops processor internal clock to save power.                                                  | page 5-4                          |
|                                                                  | STOP             | 30000008h | Disables system clocks except for those used by the RTC and the system controller for the wakeup function. | page 5-4                          |
|                                                                  | WAKEUP_CTRL      | 3000000Ch | Enables the sources used to generate the Wakeup signal.                                                    | page 5-8                          |
|                                                                  | WAKEUP_STAT      | 30000010h | Returns the status of nWakeup sources when the Wakeup signal is activated.                                 | page 5-9                          |
|                                                                  | REMAP            | 30000014h | Controls the state of the remap output and alters the system memory map.                                   | page 5-10                         |
|                                                                  | PLL_STATUS       | 30000018h | Contains the PLL locked status.                                                                            | page 5-10                         |
|                                                                  | SOFTRESET        | 3000001Ch | Generates the soft reset.                                                                                  | page 5-11                         |
|                                                                  | ASB_MODE         | 30000020h | Controls ASB mode.                                                                                         | page 5-11                         |
|                                                                  | SCRATCH          | 30000024h | Provides an 8-bit scratch register that is not cleared by reset.                                           | page 5-13                         |
|                                                                  | Reserved         | 3000002Ch | -                                                                                                          | -                                 |
|                                                                  | LOW_POWER_CONFIG | 30000030h | Low-Power configuration register.                                                                          | page 5-14                         |

**Table 6. CX24138 Register Index (2 of 20)**

| *                                                                | Register Name         | Address   | Description                          | Refer to CX2414X Document 102210B |
|------------------------------------------------------------------|-----------------------|-----------|--------------------------------------|-----------------------------------|
|                                                                  | LOW_POWER_CLK_GATE    | 30000034h | Low-Power clock gate register.       | page 5-15                         |
|                                                                  | LOW_POWER_RESET       | 30000038h | Low-Power reset register.            | page 5-16                         |
|                                                                  | HSX_MODE_BITS         | 30000060  | HSX Mode bits                        | page 5-19                         |
|                                                                  | HSX_CRITICAL_PRIORITY | 30000064  | HSX arbiter critical priority levels | page 5-21                         |
|                                                                  | RESET_WAIT_TIMER      | 30000070  | Memory reset wait timer              | page 5-23                         |
|                                                                  | PREFETCH_MONITOR      | 30000080  | R/W Prefetch Monitor                 | page 5-24                         |
|                                                                  | LOW_POWER_WAKEUP      | 3000003Ch | Low-Power wakeup timer register.     | page 5-17                         |
| <b>PCI Expansion Bus (300100xxh) – prefix: PCI_ suffix: _REG</b> |                       |           |                                      |                                   |
| *                                                                | ROM_DESC0             | 30010000h | ROM Descriptor #0                    | page 8-10                         |
| *                                                                | ROM_DESC1             | 30010004h | ROM Descriptor #1                    | page 8-11                         |
| *                                                                | ISAROM_DESC2          | 30010008h | ROM/ISA Descriptor #2                | page 8-11                         |
| *                                                                | ISAROM_DESC3          | 3001000Ch | ROM/ISA Descriptor #3                | page 8-11                         |
| *                                                                | ISA_DESC4             | 30010010h | ISA Descriptor #4                    | page 8-11                         |
| *                                                                | ISA_DESC5             | 30010014h | ISA Descriptor #5                    | page 8-11                         |
| *                                                                | ISA_DESC6             | 30010018h | ISA Descriptor #6                    | page 8-11                         |
| *                                                                | ISA_DESC7             | 3001001Ch | ISA Descriptor #7                    | page 8-11                         |
|                                                                  | ROM0_MAP              | 30010020h | ROM #0 Mapping Register              | page 8-12                         |
|                                                                  | ROM1_MAP              | 30010024h | ROM #1 Mapping Register              | page 8-12                         |
|                                                                  | ROM2_MAP              | 30010028h | ROM #2 Mapping Register              | page 8-12                         |
|                                                                  | ROM3_MAP              | 3001002Ch | ROM #3 Mapping Register              | page 8-12                         |
| *                                                                | ROM_MODE_REG          | 30010030h | ISA Mode register                    | page 8-14                         |
|                                                                  | 3B XOE_MASK           | 30010034h | XOE Mask register                    | page 8-15                         |
|                                                                  | PAGE_SIZE             | 30010038h | Flash page boundary register         | page 8-15                         |
|                                                                  | EXT_DESC0             | 30010080  | Descriptor #0 Extended Control       | page 8-16                         |
|                                                                  | EXT_DESC1             | 30010084  | Descriptor #1 Extended Control       | page 8-16                         |
|                                                                  | EXT_DESC2             | 30010088  | Descriptor #2 Extended Control       | page 8-16                         |
|                                                                  | EXT_DESC3             | 3001008C  | Descriptor #3 Extended Control       | page 8-16                         |
|                                                                  | EXT_DESC4             | 30010090  | Descriptor #4 Extended Control       | page 8-16                         |

**Table 6. CX24138 Register Index (3 of 20)**

| *                                                                  | Register Name  | Address   | Description                                  | Refer to CX2414X Document 102210B |
|--------------------------------------------------------------------|----------------|-----------|----------------------------------------------|-----------------------------------|
|                                                                    | EXT_DESC5      | 30010094  | Descriptor #5 Extended Control               | page 8-16                         |
|                                                                    | EXT_DESC6      | 30010098  | Descriptor #6 Extended Control               | page 8-16                         |
|                                                                    | EXT_DESC7      | 3001009C  | Descriptor #7 Extended Control               | page 8-16                         |
| <b>SDRAM (300700xxh) – prefix: SDR_ suffix: _REG</b>               |                |           |                                              |                                   |
|                                                                    | MEM_CFG        | 30070004h | Memory configuration register                | page 20-10                        |
|                                                                    | REF_CNT        | 30070008h | Refresh count register                       | page 20-12                        |
|                                                                    | PROC_CRIT      | 30070010h | Processor critical control register          | page 20-13                        |
|                                                                    | LOW_PWR        | 30070020h | Self Refresh Register                        | page 20-14                        |
| <b>MPEG Host Interface (304000xxh) – prefix: MPG_ suffix: _REG</b> |                |           |                                              |                                   |
|                                                                    | CONTROL0       | 30400000h | Control 0                                    | page 13-5                         |
| *                                                                  | CONTROL1       | 30400004h | Control 1                                    | page 13-7                         |
|                                                                    | COMMAND        | 30400008h | Command register                             | page 13-9                         |
|                                                                    | ISR            | 3040000Ch | Interrupt status register                    | page 13-11                        |
|                                                                    | IMR            | 30400010h | Interrupt mask register                      | page 13-12                        |
|                                                                    | ERROR_STATUS   | 30400014h | Error status register                        | page 13-13                        |
|                                                                    | ERROR_MASK     | 30400018h | Error mask register                          | page 13-13                        |
| *                                                                  | DECODE_STATUS  | 3040001Ch | Decoder status register                      | page 13-14                        |
|                                                                    | STC_HI         | 30400020h | System time clock high                       | page 13-16                        |
|                                                                    | STC_LO         | 30400024h | System time clock low                        | page 13-16                        |
|                                                                    | PSCRS_HI       | 30400028h | Program-system clock reference snapshot high | page 13-16                        |
|                                                                    | PSCRS_LO       | 3040002Ch | Program-system clock reference snapshot low  | page 13-17                        |
|                                                                    | STCS_HI        | 30400030h | System time clock snapshot high              | page 13-17                        |
|                                                                    | STCS_LO        | 30400034h | System time clock snapshot low               | page 13-17                        |
|                                                                    | PCR_TIMER_INFO | 30400038h | PCR interrupt timer                          | page 13-18                        |
|                                                                    | PTS_HI         | 3040003Ch | Audio program time stamp high                | page 13-18                        |
|                                                                    | PTS_LO         | 30400040h | Audio program time stamp low                 | page 13-19                        |
|                                                                    | PTSSC_HI       | 30400044h | Audio PTS (sample converted) high            | page 13-19                        |

**Table 6. CX24138 Register Index (4 of 20)**

| *                                                                                     | Register Name   | Address      | Description                                              | Refer to CX2414X Document 102210B |
|---------------------------------------------------------------------------------------|-----------------|--------------|----------------------------------------------------------|-----------------------------------|
|                                                                                       | PTSSC_LO        | 30400048h    | Audio PTS (sample converted) low                         | page 13-19                        |
|                                                                                       | PTS_COUNT_HI    | 3040004Ch    | Audio PTS counter high                                   | page 13-20                        |
|                                                                                       | PTS_COUNT_LO    | 30400050h    | Audio PTS counter low                                    | page 13-20                        |
|                                                                                       | PTS_TIMER_INFO  | 30400054h    | Audio PTS interrupt timer                                | page 13-21                        |
|                                                                                       | MCODE_W         | 30400058h    | Microcode memory area                                    | page 13-21                        |
|                                                                                       | VIDEO_SIZE      | 3040005Ch    | Video picture size                                       | page 13-22                        |
|                                                                                       | GOP_TIME_CODE   | 30400060h    | GOP time code                                            | page 13-22                        |
|                                                                                       | FRAME_DROP_CNT  | 30400064h    | Video frame drop/repeat counter                          | page 13-23                        |
|                                                                                       | AUDIO_DROP_CNT  | 30400068h    | Audio frame drop/repeat counter                          | page 13-23                        |
|                                                                                       | VPTS_HI         | 3040006Ch    | Video Program Time Stamp High                            | page 13-24                        |
|                                                                                       | VPTS_LO         | 30400070h    | Video Program Time Stamp Low                             | page 13-25                        |
|                                                                                       | APTS_CNT_HI@PCR | 30400074h    | Audio PTS High counter value at PCR snapshot             | page 13-25                        |
|                                                                                       | APTS_CNT_LO@PCR | 30400078h    | Audio PTS Low counter value at PCR snapshot              | page 13-25                        |
|                                                                                       | -               | 3040007C-F4h | Reserved                                                 | -                                 |
| <b>General Purpose Timer (304300xxh) – prefix: TIM_ suffix: _REG (n=timer number)</b> |                 |              |                                                          |                                   |
|                                                                                       | VALUE           | 304300n0h    | Timer counter value.                                     | page 5-37                         |
|                                                                                       | LIMIT           | 304300n4h    | Timer limit value.                                       | page 5-38                         |
|                                                                                       | MODE            | 304300n8h    | Timer mode.                                              | page 5-38                         |
|                                                                                       | -               | 304300nCh    | Reserved                                                 |                                   |
|                                                                                       | TimerIRQ        | 30430080h    | Timer interrupt bits.                                    | page 5-39                         |
| <b>General System (304400xxh) - prefix: PLL_ suffix: _REG</b>                         |                 |              |                                                          |                                   |
|                                                                                       | VID_CONFIG      | 30440000h    | Program MPEG video clock                                 | page 4-8                          |
|                                                                                       | AUD_CONFIG      | 30440004h    | Program audio clock                                      | page 4-8                          |
|                                                                                       | CPD_CONFIG      | 30440008h    | Program ARM clock                                        | page 4-8                          |
|                                                                                       | MEM_CONFIG      | 3044000Ch    | Program memory clock                                     | page 4-9                          |
|                                                                                       | BYPASS_OPT      | 30440010h    | Clock source control                                     | page 4-9                          |
|                                                                                       | RTC_DIVIDER     | 30440014h    | Divider value used to produce the real time clockcounter | page 4-11                         |

**Table 6. CX24138 Register Index (5 of 20)**

| *                                                                   | Register Name    | Address   | Description                                     | Refer to CX2414X Document 102210B |
|---------------------------------------------------------------------|------------------|-----------|-------------------------------------------------|-----------------------------------|
|                                                                     | DIV1             | 30440018h | Divider value for the clock domains             | page 4-11                         |
|                                                                     | DIV2             | 3044001C  | Divider value for the clock domains             | page 4-12                         |
|                                                                     | PLL_CONFIG0      | 30440020  | Values of configuration inputs 0-31             | page 4-13                         |
|                                                                     | PLL_CONFIG1      | 30440024  | Value of configuration input 32                 |                                   |
|                                                                     | USB_CONFIG       | 3044002C  | Program USB clock                               | page 4-15                         |
|                                                                     | MEM_DELAY        | 30440030h | Memory Control input/output delay               | page 4-15                         |
|                                                                     | PIN_MUXSEL_REG   | 30440034h | PIO pin muxing selects                          | page 4-16                         |
|                                                                     | PIN_PIO_MUX0     | 30440050h | PIO [31:0] alternate function pin mux selects   | page 4-20                         |
|                                                                     | PIN_PIO_MUX1     | 30440054h | PIO[63:32] alternate function pin mux selects   | page 4-21                         |
|                                                                     | PIN_PIO_MUX2     | 30440058h | PIO[95:64] alternate function pin mux selects   | page 4-23                         |
|                                                                     | PIN_PIO_MUX3_REG | 3044005Ch | PIO Pin Mux 3 Select register                   | page 4-24                         |
|                                                                     | PLL_LOCKCMD      | 30440038h | Resource lock command register                  | page 4-18                         |
|                                                                     | PLL_LOCKSTAT     | 3044003Ch | Resource lock status register                   | page 4-18                         |
|                                                                     | CLK_TREE_SEL     | 30440064  | Selects source PLL for derivation clock trees.  | page 4-26                         |
|                                                                     | PLL_PRESCALE     | 30440068  | Selects Prescale values for PLL reference clock | page 4-27                         |
|                                                                     | TEST_REG         | 30440070  | For test only                                   | page 4-28                         |
| <b>Interrupt Controller (304500xxh) – prefix: ITC_ suffix: _REG</b> |                  |           |                                                 |                                   |
|                                                                     | INTDEST          | 30450000h | Interrupt destination register                  | page 5-29                         |
|                                                                     | INTENABLE        | 30450004h | Interrupt enable masking register               | page 5-30                         |
|                                                                     | INTRIRQ          | 30450008h | Interrupt request IRQ register                  | page 5-30                         |
|                                                                     | INTRFIQ          | 3045000Ch | Interrupt request FIQ register                  | page 5-31                         |
|                                                                     | INTSTATCLR       | 30450010h | Interrupt status/clear register                 | page 5-32                         |
|                                                                     | INTSTATSET       | 30450014h | Interrupt status/set register                   | page 5-33                         |
|                                                                     | Register Name    | Address   | Description                                     | Refer to CX1414X                  |
|                                                                     | EXPENABLE        | 304500020 | Expansion Enable Register                       | page 5-34                         |
|                                                                     | EXPSTATCLR       | 304500024 | Expansion Status/Clear Register                 | page 5-34                         |
|                                                                     | EXPSTATSET       | 304500028 | Expansion Status/Set Register                   | page 5-35                         |

**Table 6. CX24138 Register Index (6 of 20)**

| *                                                                     | Register Name         | Address   | Description                                     | Refer to CX2414X Document 102210B |
|-----------------------------------------------------------------------|-----------------------|-----------|-------------------------------------------------|-----------------------------------|
| <b>Display Refresh Module (304600xxh) – prefix: DRM_ suffix: _REG</b> |                       |           |                                                 |                                   |
|                                                                       | CONTROL               | 30460000h | DRM control                                     | page 10-29                        |
|                                                                       | INTERRUPT_ENABLE      | 30460004h | DRM interrupt enable                            | page 10-31                        |
|                                                                       | STATUS                | 30460008h | DRM status (read only / interrupt status reset) | page 10-32                        |
|                                                                       | OSD_POINTER           | 3046000Ch | OSD pointer                                     | page 10-33                        |
|                                                                       | COLOR_KEY             | 30460010h | Color key compare value                         | page 10-34                        |
|                                                                       | GRAPHICS_BORDER_COLOR | 30460014h | Graphics background color                       | page 10-35                        |
|                                                                       | DWI_CONTROL1          | 30460018h | DWI control 1                                   | page 10-35                        |
|                                                                       | DWI_CONTROL2          | 3046001Ch | DWI control 2                                   | page 10-36                        |
|                                                                       | SCREEN_START          | 30460020h | Screen start position                           | page 10-37                        |
|                                                                       | SCREEN_END            | 30460024h | Screen end position                             | page 10-37                        |
|                                                                       | CONTROL 2             | 3046002Ch | DRM Control 2                                   | page 10-38                        |
|                                                                       | MPEG_OFFSET_WIDTH     | 30460030h | MPEG address offset and fetched width           | page 10-39                        |
|                                                                       | MPEG_VERTICAL_OFFSET  | 30460034h | MPEG vertical cropping offset                   | page 10-40                        |
|                                                                       | MPEG_POSITION         | 30460038h | MPEG starting screen X and Y position           | page 10-41                        |
|                                                                       | MPEG_SIZE             | 3046003Ch | MPEG screen height and width                    | page 10-42                        |
|                                                                       | MPEG_X_INC            | 30460040h | MPEG X increment                                | page 10-42                        |
|                                                                       | MPEG_Y_INC            | 30460044h | MPEG Y increment                                | page 10-44                        |
|                                                                       | DRM_SHARP             | 30460048h | DRM Sharpening filter coefficients              | page 10-44                        |
|                                                                       | DWI_CONTROL3_REG      | 3046004Ch | DWI controls                                    | page 10-45                        |
|                                                                       | VBI_BUF_0             | 30460050h | External VBI buffer 0 address                   | page 10-46                        |
|                                                                       | VBI_BUF_1             | 30460054h | External VBI buffer 1 address                   | page 10-46                        |
|                                                                       | VID_BUF_0             | 30460058h | External video buffer 0 address                 | page 10-47                        |
|                                                                       | VID_BUF_1             | 3046005Ch | External video buffer 1 address                 | page 10-47                        |
|                                                                       | VID_BUF_2             | 30460060h | External video buffer 2 address                 | page 10-48                        |
|                                                                       | VID_POSITION          | 30460064h | External video starting screen X and Y position | page 10-48                        |
|                                                                       | VID_SIZE              | 30460068h | External video screen height and width          | page 10-49                        |
|                                                                       | VID_STRIDE            | 3046006Ch | External video stride and VBI line start        | page 10-49                        |

**Table 6. CX24138 Register Index (7 of 20)**

| * | Register Name        | Address      | Description                                            | Refer to CX2414X Document 102210B |
|---|----------------------|--------------|--------------------------------------------------------|-----------------------------------|
|   | TELETEXT_STRIDE      | 30460070h    | Teletext line stride and line disable                  | page 10-50                        |
|   | TELETEXT_FIELD1      | 30460074h    | Active teletext lines for field 1                      | page 10-51                        |
|   | TELETEXT_FIELD2      | 30460078h    | Active teletext lines for field 2                      | page 10-52                        |
|   | TELETEXT_FIELD1_ADDR | 3046007Ch    | Teletext field 1 address                               | page 10-53                        |
|   | TELETEXT_FIELD2_ADDR | 30460080h    | Teletext field 2 address                               | page 10-53                        |
|   | CURSOR_CONTROL       | 30460084h    | Cursor control                                         | page 10-54                        |
|   | CURSOR_STORE_ADDR    | 30460088h    | Cursor store address                                   | page 10-55                        |
|   | CURSOR_PALETTE_0     | 3046008Ch    | Cursor palette 0                                       | page 10-55                        |
|   | CURSOR_PALETTE_1     | 30460090h    | Cursor palette 1                                       | page 10-56                        |
|   | CURSOR_PALETTE_2     | 30460094h    | Cursor palette 2                                       | page 10-56                        |
|   | CURSOR_FETCH_SIZE    | 30460098h    | Cursor Fetch Size                                      | page 10-57                        |
|   | MPEG_SCALING_COEFF   | 3046009Ch    | MPEG Scaling Coefficients (Video channels 0 & 1)       | page 10-57                        |
|   | MPEG_STILL_CNTL      | 304600A0h    | MPEG control for SW still (Video Channel 0)            | page 10-58                        |
|   | MPEG_LUMA_ADDR       | 304600A4h    | MPEG Luma Address for SW still (Video Channel 0)       | page 10-59                        |
|   | MPEG_CHROMA_ADDR     | 304600A8h    | MPEG Chroma Address for SW still (Video Channel 0)     | page 10-60                        |
|   | MPEG_HEIGHT/WIDTH    | 304600ACH    | MPEG Height and Width for SW still (Video Channel 0)   | page 10-60                        |
|   | MPEG_WIPE_LUMA       | 304600B0h    | MPEG Luma Address for Wipe function (VideoChannel 0)   | page 10-61                        |
|   | MPEG_WIPE_CHROMA     | 304600B4h    | MPEG Chroma Address for Wipe function (VideoChannel 0) | page 10-62                        |
|   | MPEG_TILE_PARMs      | 304600B8h    | MPEG Tile Parameters (Video Channel 0)                 | page 10-62                        |
|   | -                    | 304600BC-CCh | Reserved for future expansion                          | -                                 |
|   | MPEG_OFFSET_WIDTH    | 304600D0h    | MPEG address offset and fetched width (VideoChannel 1) | page 10-39                        |
|   | MPEG_VERTICAL_OFFSET | 304600D4h    | MPEG vertical offset (Video Channel 1)                 | page 10-40                        |
|   | MPEG_POSITION        | 304600D8h    | MPEG starting screen X and Y position (VideoChannel 1) | page 10-41                        |

**Table 6. CX24138 Register Index (8 of 20)**

| * | Register Name     | Address   | Description                                                       | Refer to CX2414X Document 102210B |
|---|-------------------|-----------|-------------------------------------------------------------------|-----------------------------------|
|   | MPEG_SIZE         | 304600DCh | MPEG screen height and width (Video Channel 1)                    | page 10-42                        |
|   | MPEG_X_INC        | 304600E0h | MPEG X increment (Video Channel 1)                                | page 10-42                        |
|   | MPEG_Y_INC        | 304600E4h | MPEG Y increment (Video Channel 1)                                | page 10-44                        |
|   | DRM_SHARP         | 304600E8h | DRM Sharpening filter coefficients (Video Channel1)               | page 10-44                        |
|   | -                 | 304600ECh | Reserved for future expansion                                     | -                                 |
|   | VBI_BUF_0         | 304600F0h | External VBI Buffer 0 address (Video Channel 1)                   | page 10-46                        |
|   | VBI_BUF_1         | 304600F4h | External VBI Buffer 1 address (Video Channel 1)                   | page 10-46                        |
|   | VID_BUF_0         | 304600F8h | External Video Buffer 0 address (Video Channel 1)                 | page 10-47                        |
|   | VID_BUF_1         | 304600FCh | External Video Buffer 1 address (Video Channel 1)                 | page 10-47                        |
|   | VID_BUF_2         | 30460100h | External Video Buffer 2 address (Video Channel 1)                 | page 10-48                        |
|   | VID_POSITION      | 30460104h | External Video starting screen X and Y position (Video Channel 1) | page 10-48                        |
|   | VID_SIZE          | 30460108h | External Video screen height and width (VideoChannel 1)           | page 10-49                        |
|   | VID_STRIDE        | 3046010Ch | External Video stride and VBI line start (VideoChannel 1)         | page 10-49                        |
|   | MPEG_STILL_CNTL   | 30460110h | MPEG control for SW still (Video Channel 1)                       | page 10-58                        |
|   | MPEG_LUMA_ADDR    | 30460114h | MPEG Luma Address for SW still (Video Channel 1)                  | page 10-59                        |
|   | MPEG_CHROMA_ADDR  | 30460118h | MPEG Chroma Address for SW still (Video Channel1)                 | page 10-60                        |
|   | MPEG_HEIGHT/WIDTH | 3046011Ch | MPEG Height and Width for SW still (Video Channel1)               | page 10-60                        |
|   | MPEG_WIPE_LUMA    | 30460120h | MPEG Luma Address for Wipe function (VideoChannel 1)              | page 10-61                        |
|   | MPEG_WIPE_CHROMA  | 30460124h | MPEG Chroma Address for Wipe function (VideoChannel 1)            | page 10-62                        |

**Table 6. CX24138 Register Index (9 of 20)**

| *                                                                  | Register Name     | Address        | Description                                            | Refer to CX2414X Document 102210B |
|--------------------------------------------------------------------|-------------------|----------------|--------------------------------------------------------|-----------------------------------|
|                                                                    | MPEG_TILE_PARMS   | 30460128h      | MPEG Tile Parameters (Video Channel 1)                 | page 10-62                        |
|                                                                    | VIDEO_ALPHA       | 3046012Ch      | Video Alpha Values                                     | page 10-63                        |
|                                                                    | SATURATION_VALUES | 30460130h      | Saturation Values                                      | page 10-64                        |
|                                                                    | -                 | 30460134h-158h | Reserved for future expansion                          | -                                 |
|                                                                    | VID0_LUMA_ADDR    | 30460140       | Video CH0 Current Luma address reg                     | page 10-64                        |
|                                                                    | VID0_CHROMA_ADDR  | 30460144       | Video CH0 Current Chroma address reg                   | page 10-65                        |
|                                                                    | VID1_LUMA_ADDR    | 30460148       | Video CH1 Current Luma address reg                     | page 10-64                        |
|                                                                    | VID1_CHROMA_ADDR  | 3046014C       | Video CH1 Current Chroma address reg                   | page 10-65                        |
|                                                                    | SAR               | 30460160h      | Signature analysis register                            | page 10-66                        |
| <b>General Purpose I/O (304700xxh) – prefix: GPI_ suffix: _REG</b> |                   |                |                                                        |                                   |
|                                                                    | READ              | 30470004h      | Current value of PIO[31:0] pins (inputs and outputs).  | page 7-9                          |
|                                                                    | DRIVE_HIGH        | 30470008h      | Configure PIO[31:0] pins as outputs and drive high.    | page 7-10                         |
|                                                                    | DRIVE_LOW         | 30470010h      | Configure PIO[31:0] pins as outputs and drive low.     | page 7-11                         |
|                                                                    | DRIVE_OFF         | 30470014h      | Configure PIO[31:0] pins as inputs.                    | page 7-12                         |
|                                                                    | IRQ_STATUS        | 30470020h      | Interrupt status request for PIO[31:0] pins.           | page 7-13                         |
|                                                                    | IRQ_ENABLE        | 30470024h      | Enable interrupt request for PIO[31:0] pins.           | page 7-14                         |
|                                                                    | POS_EDGE          | 30470028h      | Interrupt on rising edge of PIO[31:0] pin.             | page 7-15                         |
|                                                                    | NEG_EDGE          | 3047002Ch      | Interrupt on falling edge of PIO[31:0] pin.            | page 7-16                         |
|                                                                    | READ              | 30470034h      | Current value of PIO[63:32] pins (inputs and outputs). | page 7-9                          |
|                                                                    | DRIVE_HIGH        | 30470038h      | Configure PIO[63:32] pins as outputs and drive high.   | page 7-10                         |
|                                                                    | DRIVE_LOW         | 30470040h      | Configure PIO[63:32] pins as outputs and drive low.    | page 7-11                         |
|                                                                    | DRIVE_OFF         | 30470044h      | Configure PIO[63:32] pins as inputs.                   | page 7-12                         |
|                                                                    | IRQ_STATUS        | 30470050h      | Interrupt status request for PIO[63:32] pins.          | page 7-13                         |
|                                                                    | IRQ_ENABLE        | 30470054h      | Enable interrupt request for PIO[63:32] pins.          | page 7-14                         |

**Table 6. CX24138 Register Index (10 of 20)**

| *                                                              | Register Name | Address   | Description                                             | Refer to CX2414X Document 102210B |
|----------------------------------------------------------------|---------------|-----------|---------------------------------------------------------|-----------------------------------|
|                                                                | POS_EDGE      | 30470058h | Interrupt on rising edge of PIO[63:32] pin.             | page 7-15                         |
|                                                                | NEG_EDGE      | 3047005Ch | Interrupt on falling edge of PIO[63:32] pin.            | page 7-16                         |
|                                                                | READ          | 30470064h | Current value of PIO[95:64] pins (inputs and outputs).  | page 7-9                          |
|                                                                | DRIVE_HIGH    | 30470068h | Configure PIO[95:64] pins as outputs and drive high.    | page 7-10                         |
|                                                                | DRIVE_LOW     | 30470070h | Configure PIO[95:64] pins as outputs and drive low.     | page 7-11                         |
|                                                                | DRIVE_OFF     | 30470074h | Configure PIO[95:64] pins as inputs.                    | page 7-12                         |
|                                                                | IRQ_STATUS    | 30470080h | Interrupt status request for PIO[95:64] pins.           | page 7-13                         |
|                                                                | IRQ_ENABLE    | 30470084h | Enable interrupt request for PIO[95:64] pins.           | page 7-14                         |
|                                                                | POS_EDGE      | 30470088h | Interrupt on rising edge of PIO[95:64] pin.             | page 7-15                         |
|                                                                | NEG_EDGE      | 3047008Ch | Interrupt on falling edge of PIO[95:64] pin.            | page 7-16                         |
|                                                                | READ          | 30470094h | Current value of PIO[127:96] pins (inputs and outputs). | page 7-9                          |
|                                                                | DRIVE_HIGH    | 30470098h | Configure PIO[127:96] pins as outputs and drive high.   | page 7-10                         |
|                                                                | DRIVE_LOW     | 304700A0h | Configure PIO[127:96] pins as outputs and drive low.    | page 7-11                         |
|                                                                | DRIVE_OFF     | 304700A4h | Configure PIO[127:96] pins as inputs.                   | page 7-12                         |
|                                                                | IRQ_STATUS    | 304700B0h | Interrupt status request for PIO[127:96] pins.          | page 7-13                         |
|                                                                | IRQ_ENABLE    | 304700B4h | Enable interrupt request for PIO[127:96] pins.          | page 7-14                         |
|                                                                | POS_EDGE      | 304700B8h | Interrupt on rising edge of PIO[127:96] pin.            | page 7-15                         |
|                                                                | NEG_EDGE      | 304700BCh | Interrupt on falling edge of PIO[127:96] pin.           | page 7-16                         |
|                                                                | LEVEL         | 304700C0h | Interrupt on level if no edge and enabled               | page 7-17                         |
| <b>Real Time Clock (304F10xxh) – prefix: RTC_ suffix: _REG</b> |               |           |                                                         |                                   |
|                                                                | DATA          | 30490000h | RTC data register                                       | page 15-2                         |
|                                                                | MATCH         | 30490004h | RTC match register                                      | page 15-2                         |
|                                                                | EOI           | 30490008h | RTC end of interrupt                                    | page 15-2                         |

**Table 6. CX24138 Register Index (11 of 20)**

| *                                                       | Register Name | Address             | Description                                                                                                                                | Refer to CX2414X Document 102210B |
|---------------------------------------------------------|---------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| <b>Graphics Accelerator – prefix: GXA_ suffix: _REG</b> |               |                     |                                                                                                                                            |                                   |
|                                                         | PARAMETER0    | 304A0000            | First parameter of a command. This is a register RWview of the parameter which is normally sent as part of a command not as a register RW. |                                   |
|                                                         | PARAMETER1    | 304A0004            | Second parameter of a command.                                                                                                             |                                   |
|                                                         | PARAMETER2    | 304A0008            | Third parameter of a command.                                                                                                              |                                   |
|                                                         | Reserved      | 304A000C - 304A0018 | Reserved                                                                                                                                   |                                   |
|                                                         | CMD           | 304A001C            | GXA Command Register                                                                                                                       | page 9-14                         |
|                                                         | FG_COLOR      | 304A0020            | Foreground Color Register                                                                                                                  | page 9-15                         |
|                                                         | BG_COLOR      | 304A0024            | Background Color Register                                                                                                                  | page 9-15                         |
|                                                         | LINE_PATT     | 304A0028            | Line Pattern Register                                                                                                                      | page 9-16                         |
|                                                         | DST_XY_INC    | 304A002C            | Destination XY Increment Register                                                                                                          | page 9-16                         |
|                                                         | CFG           | 304A0030            | GXA Configuration Register                                                                                                                 | page 9-17                         |
|                                                         | BLT_CONTROL   | 304A0034            | Blit Control (Direction) Register                                                                                                          | page 9-19                         |
|                                                         | LINE_CONTROL  | 304A0038            | LINE Control Register                                                                                                                      | page 9-20                         |
|                                                         | Reserved      | 304A003C            | Reserved                                                                                                                                   | -                                 |
|                                                         | BMAP0_TYPE    | 304A0040            | Bitmap Type Register                                                                                                                       | page 9-21                         |
|                                                         | BMAP0_ADDR    | 304A0044            | Bitmap Address Registers                                                                                                                   | page 9-21                         |
|                                                         | BMAP1_TYPE    | 304A0048            | Bitmap Type Registers                                                                                                                      | page 9-21                         |
|                                                         | BMAP1_ADDR    | 304A004C            | Bitmap Address Registers                                                                                                                   | page 9-21                         |
|                                                         | BMAP2_TYPE    | 304A0050            | Bitmap Type Registers                                                                                                                      | page 9-21                         |
|                                                         | BMAP2_ADDR    | 304A0054            | Bitmap Address Registers                                                                                                                   | page 9-21                         |
|                                                         | BMAP3_TYPE    | 304A0058            | Bitmap Type Registers                                                                                                                      | page 9-21                         |
|                                                         | BMAP3_ADDR    | 304A005C            | Bitmap Address Registers                                                                                                                   | page 9-21                         |
|                                                         | BMAP4_TYPE    | 304A0060            | Bitmap Type Registers                                                                                                                      | page 9-21                         |
|                                                         | BMAP4_ADDR    | 304A0064            | Bitmap Address Registers                                                                                                                   | page 9-21                         |
|                                                         | BMAP5_TYPE    | 304A0068            | Bitmap Type Registers                                                                                                                      | page 9-21                         |
|                                                         | BMAP5_ADDR    | 304A006C            | Bitmap Address Registers                                                                                                                   | page 9-21                         |

**Table 6. CX24138 Register Index (12 of 20)**

| *                                                        | Register Name    | Address               | Description                           | Refer to CX2414X Document 102210B |
|----------------------------------------------------------|------------------|-----------------------|---------------------------------------|-----------------------------------|
|                                                          | BMAP6_TYPE       | 304A0070              | Bitmap Type Registers                 | page 9-21                         |
|                                                          | BMAP6_ADDR       | 304A0074              | Not implemented                       | page 9-21                         |
|                                                          | BMAP7_TYPE       | 304A0078              | Bitmap Type Registers                 | page 9-21                         |
|                                                          | BMAP7_ADDR       | 304A007C              | Not implemented                       | page 9-21                         |
|                                                          | BRES0_ADDR       | 304A0080              | Bresenham 0, Address Register         | page 9-22                         |
|                                                          | BRES0_ERR        | 304A0084              | Bresenham 0, Error, Register          | page 9-23                         |
|                                                          | BRES0_K1         | 304A0088              | Bresenham 0, K1 Register              | page 9-23                         |
|                                                          | BRES0_K2         | 304A008C              | Bresenham 0, K2 Register              | page 9-23                         |
|                                                          | BRES0_INC1       | 304A0090              | Bresenham 0, Increment 1 Register     | page 9-24                         |
|                                                          | BRES0_INC2       | 304A0094              | Bresenham 0, Increment 1 Register     | page 9-24                         |
|                                                          | BRES0_LENGTH     | 304A0098              | Bresenham 0, Length Register          | page 9-25                         |
|                                                          | Reserved         | 304A009C - 304A00A8   | Reserved for Bresenham 1              | -                                 |
|                                                          | Reserved         | 304A00AC - 304A00EC   |                                       | -                                 |
|                                                          | DEPTH            | 304A00F4              | See "GXA Depth Register" on page 25.  | page 9-25                         |
|                                                          | CFG2             | 304A00FC              | See "GXA Configuration 2 Register     | "page 9-26                        |
| <b>High-Speed Data Port – prefix: HSDP_ suffix: _REG</b> |                  |                       |                                       |                                   |
|                                                          | -                | 304CC000h             | Reserved                              | -                                 |
|                                                          | -                | 304CC004h             | Reserved                              | -                                 |
| *                                                        | TSC_PORT_CNTL    | 304CC008h             | HSDP 0 register                       | page 14-11                        |
|                                                          | -                | 304CC00Ch - 304CC01Ch | Reserved                              | -                                 |
| *                                                        | SP_INPUT_CNTL    | 304CC020h             | Demux input selection                 | page 14-14                        |
|                                                          | -                | 304CC024h             | Reserved                              | -                                 |
| *                                                        | TS_PKT_CNTL      | 304CC040h             | Transport Stream packet control       | page 14-15                        |
| *                                                        | TS_ERR_STATUS    | 304CC048h             | Transport Stream error control        | page 14-16                        |
| *                                                        | TSC_GEN_CLK_CNTL | 304CC058h             | Bi-Di port 0 clock generation control | page 14-17                        |

**Table 6. CX24138 Register Index (13 of 20)**

| *                                                    | Register Name               | Address   | Description                                       | Refer to CX2414X Document 102210B |
|------------------------------------------------------|-----------------------------|-----------|---------------------------------------------------|-----------------------------------|
| <b>TV Encoder (304D00xxh) – prefix: suffix: _REG</b> |                             |           |                                                   |                                   |
|                                                      | DAC Status                  | 304D0000h | DAC status and other status bits                  | page 23-32                        |
|                                                      | Reset                       | 304D0004h | Resets                                            | page 23-33                        |
|                                                      | Line Time                   | 304D0010h | Horizontal line time                              | page 23-33                        |
|                                                      | Horizontal Timing           | 304D0014h | Horizontal burst and analog H sync width          | page 23-34                        |
|                                                      | H Blank                     | 304D0018h | Horizontal blank and vertical active region       | page 23-34                        |
|                                                      | H Sync                      | 304D001Ch | Horizontal sync and vertical blank                | page 23-35                        |
|                                                      | Control0                    | 304D0020h | Status and control bits                           | page 23-36                        |
|                                                      | Amplitude                   | 304D0024h | Various pulse amplitudes                          | page 23-38                        |
|                                                      | YUV Multiplication Factor   | 304D0028h | Multiplication Factors for YUV components         | page 23-39                        |
|                                                      | YCrCb Multiplication Factor | 304D002Ch | Multiplication Factors for YCrCb components       | page 23-40                        |
|                                                      | Dr for SECAM                | 304D0030h | Subcarrier Increment for PAL/NTSC or Dr for SECAM | page 23-40                        |
|                                                      | Db for SECAM                | 304D0034h | Db for SECAM                                      | page 23-41                        |
|                                                      | Dr Range                    | 304D0038h | Upper and lower boundaries for Dr                 | page 23-41                        |
|                                                      | Db Range                    | 304D003Ch | Upper and lower boundaries for Db                 | page 23-41                        |
|                                                      | Hue and Brightness Cntl     | 304D0040h | Hue and brightness control                        | page 23-42                        |
|                                                      | Chroma Control              | 304D0044h | Defines Chrominance Multipliers                   | page 23-43                        |
|                                                      | CC Control                  | 304D0048h | closed caption start                              | page 23-43                        |
|                                                      | XDS Data                    | 304D004Ch | extended data services                            | page 23-44                        |
|                                                      | CC Data                     | 304D0050h | closed caption, data bytes                        | page 23-44                        |
|                                                      | XDS/CC Control              | 304D0054h | extended data service and closed caption          | page 23-45                        |
|                                                      | WS Data                     | 304D0058h | Wide screen signaling data                        | page 23-47                        |
|                                                      | TTX Req Control             | 304D005Ch | teletext request rising                           | page 23-47                        |
|                                                      | TTX F1 Control              | 304D0060h | teletext start and end line for field 1           | page 23-48                        |
|                                                      | TTX F2 Control              | 304D0064h | teletext start and end line for field 2           | page 23-48                        |
|                                                      | TTX Line Control            | 304D0068h | teletext enable and line disables                 | page 23-49                        |

**Table 6. CX24138 Register Index (14 of 20)**

| *                                                     | Register Name             | Address       | Description                       | Refer to CX2414X Document 102210B |
|-------------------------------------------------------|---------------------------|---------------|-----------------------------------|-----------------------------------|
| <b>Demodulator (304E00xxh) – prefix: suffix: _REG</b> |                           |               |                                   |                                   |
|                                                       | DEMOD_VERSION_RESET_REG   | 304E0000h     | Demod Version Reset Register      | page 22-92                        |
|                                                       | PLL_REG1                  | 304E0004h     | PLL Register 1                    | page 22-49                        |
|                                                       | MODE_REG1                 | 304E0008h     | Mode Register 1                   | page 22-50                        |
|                                                       | MPEG_OUTPUT_CNTRL1        | 304E0010h     | MPEG Output Control 1             | page 22-50                        |
|                                                       | MPEG_OUTPUT_CNTRL2        | 304E0014h     | MPEG Output Control 2             | page 22-52                        |
|                                                       | MPEG_OUTPUT_CNTRL3        | 304E0018h     | MPEG Output Control 3             | page 22-53                        |
|                                                       | SYMBOL_RATE1              | 304E0020h     | Symbol Rate 1                     | page 22-54                        |
|                                                       | SYMBOL_RATE2&3            | 304E0024h-28h | Symbol Rate 2 & 3                 | page 22-54                        |
|                                                       | DEMOD_NOMINAL_FREQ1       | 304E002Ch     | Demod Nominal Frequency 1         | page 22-54                        |
|                                                       | DEMOD_NOMINAL_FREQ2       | 304E0030h     | Demod Nominal Frequency 2         | page 22-55                        |
|                                                       | NUMBER_OF_BINS_REG        | 304E0034h     | Number of Bins Register           | page 22-56                        |
|                                                       | VITERBI_NOMINAL           | 304E0038h     | Viterbi Nominal                   | page 22-56                        |
|                                                       | AUTO_ACQ_CODE_RATE_ENABLE | 304E003Ch     | Auto Acquisition Code Rate Enable | page 22-57                        |
|                                                       | AUTO_ACQ_CONTROL          | 304E0040h     | Viterbi Acquisition Control       | page 22-57                        |
|                                                       | SYNC_STATUS               | 304E0050h     | Sync Status                       | page 22-58                        |
|                                                       | DEMOD_CURR_CENTRAL_FREQ1  | 304E0054h     | Demod Current Central Frequency 1 | page 22-59                        |
|                                                       | DEMOD_CURR_CENTRAL_FREQ2  | 304E0058h     | Demod Current Central Frequency 2 | page 22-59                        |
|                                                       | ESNO_START/STATUS         | 304E005Ch     | Esno Start/Status Register        | page 22-60                        |
|                                                       | DEMOD_ESNO_ESTIMATE1&2    | 304E0060-64   | Demod ESNO Estimate 1 & 2         | page 22-60                        |
|                                                       | VITERBI_STATUS1           | 304E0068h     | Viterbi Status 1                  | page 22-61                        |
|                                                       | VITERBI_STATUS2           | 304E006Ch     | Viterbi Status 2                  | page 22-61                        |
|                                                       | RS_STATUS1                | 304E0070h     | RS Status 1                       | page 22-62                        |
|                                                       | RS_STATUS2 & 3            | 304E0074h-78h | RS Status 2 & 3                   | page 22-63                        |
|                                                       | TUNER_CTRL                | 304E0080h     | Tuner Control                     | page 22-64                        |
|                                                       | TUNER_CONTROL2            | 304E0084h     | Tuner Control 2                   | page 22-65                        |
|                                                       | TUNER_CONTROL3            | 304E0088h     | Tuner Control 3                   | page 22-65                        |

**Table 6. CX24138 Register Index (15 of 20)**

| * | Register Name             | Address       | Description                           | Refer to CX2414X Document 102210B |
|---|---------------------------|---------------|---------------------------------------|-----------------------------------|
|   | TUNER_SER_INT_CONTROL     | 304E008Ch     | Tuner Serial Interface Control        | page 22-66                        |
|   | TUNER_SER_INT_DATA1_2_3   | 304E0090h-98h | Tuner Serial Interface Data 1, 2, & 3 | page 22-66                        |
|   | FILTER_SD_CONTROL1        | 304E009Ch     | Filter SD Control 1                   | page 22-67                        |
|   | FILTER_SD_CONTROL2        | 304E00A0h     | Filter SD Control 2                   | page 22-67                        |
|   | LNB_CONTROL1              | 304E00A4h     | LNB Control 1                         | page 22-68                        |
|   | LNB_CONTROL2              | 304E00A8h     | LNB Control 2                         | page 22-69                        |
|   | LNB_CONTROL3              | 304E00ACh     | LNB Control 3                         | page 22-70                        |
|   | LNB_MESSAGE 1             | 304E00B0h     | LNB_MESSAGE 1                         | page 22-70                        |
|   | LNB_MESSAGE 2             | 304E00B4h     | LNB_MESSAGE 2                         | page 22-71                        |
|   | LNB_MESSAGE 3             | 304E00B8h     | LNB_MESSAGE 3                         | page 22-72                        |
|   | LNB_MESSAGE 4             | 304E00BCh     | LNB_MESSAGE 4                         | page 22-72                        |
|   | LNB_MESSAGE 5             | 304E00C0h     | LNB Message 5                         | page 22-73                        |
|   | LNB_MESSAGE 6             | 304E00C4h     | LNB Message 6                         | page 22-73                        |
|   | LNB_RECEIVER_CNTRL        | 304E00C8h     | LNB_RECEIVER_CNTRL                    | page 22-73                        |
|   | INTERRUPT_ENB_REG         | 304E00CCh     | Interrupt Enable Register             | page 22-92                        |
|   | INTERRUPT_PENDING_REG     | 304E00D0h     | Interrupt Pending Register            | page 22-93                        |
|   | LNB_AMPLITUDE_CNTRL       | 304E00D4h     | LNB Amplitude Control                 | page 22-74                        |
|   | LNB_SWITCH_MODE_CNTRL     | 304E00D8h     | LNB Switch Mode Control               | page 22-75                        |
|   | LNB_DISEQC_TONE_CNTRL     | 304E00DCh     | LNB DiSEqC Tone Control               | page 22-75                        |
|   | LNB_DISEQC_TONE_WINDOW    | 304E00E0h     | LNB DiSEqC Tone Window                | page 22-76                        |
|   | LNB_DISEQC_TONE_THRESHOLD | 304E00E4h     | LNB DiSEqC Tone Threshold             | page 22-94                        |
|   | DEMOD_ACCUM_CNTRL         | 304E00E8h     | Demod Accumulators Control            | page 22-95                        |
|   | DEMOD_ACCUM               | 304E00ECh     | Demod Accumulators                    | page 22-97                        |
|   | DEMOD_RST_ACCUM           | 304E00F0h     | Demod Reset Accumulators              | page 22-97                        |
|   | AAGC_THRESH               | 304E00F4h     | AAGC Threshold                        | page 22-76                        |
|   | AAGC_CNTL                 | 304E00F8h     | AAGC Control                          | page 22-77                        |
|   | AFC_THRESH                | 304E00FCh     | AFC Threshold                         | page 22-77                        |

**Table 6. CX24138 Register Index (16 of 20)**

| *                                                                                    | Register Name       | Address        | Description                        | Refer to CX2414X Document 102210B |
|--------------------------------------------------------------------------------------|---------------------|----------------|------------------------------------|-----------------------------------|
|                                                                                      | CTL_CONTROL_REG     | 304E0100h      | CTL Control                        | page 22-78                        |
|                                                                                      | CTL_GAIN_CONTROL    | 304E0104h      | CTL Gain Control                   | page 22-78                        |
|                                                                                      | LOCK_BTL_BW_CONTROL | 304E0108h      | Lock/BTL BW Control                | page 22-79                        |
|                                                                                      | DEMODO_PARAM        | 304E010Ch      | Demod Parameters                   | page 22-97                        |
|                                                                                      | CST_REG             | 304E0110h      | Constellation Register             | page 22-98                        |
|                                                                                      | SYMBOL_RATE_EST     | 304E0114h      | Symbol Rate Estimation             | page 22-80                        |
|                                                                                      | SYM_RATE_EST_UPDATE | 304E0118h      | Symbol Rate Estimation Update      | page 22-80                        |
|                                                                                      | SYM_COUNT_READY     | 304E011Ch      | Symbol Count Ready                 | page 22-80                        |
|                                                                                      | VIT_NORM_THRESH     | 304E0120h      | Viterbi Normalization Threshold    | page 22-81                        |
|                                                                                      | VIT_WINDOW          | 304E0128h-148h | Viterbi Window                     | page 22-81                        |
|                                                                                      | RS_PARAM1           | 304E0154h      | RS Parameters 1                    | page 22-82                        |
|                                                                                      | RS_PARAM2           | 304E0158h      | RS Parameters 2                    | page 22-83                        |
|                                                                                      | RS_PARAM3           | 304E015Ch      | RS Parameters 3                    | page 22-84                        |
|                                                                                      | OUTPUT_CNTRL        | 304E0160h      | Output Control                     | page 22-84                        |
|                                                                                      | SMOOTH_CLK_CNTRL    | 304E0164h      | Smooth Clock Control               | page 22-86                        |
|                                                                                      | ACQ_CNTRL1          | 304E0168h      | Acquisition Control 1              | page 22-86                        |
|                                                                                      | ACQ_CNTRL2          | 304E016C       | Acquisition Control 2              | page 22-87                        |
|                                                                                      | AFC_EXP_WINDOW      | 304E0170h      | AFC Expiration Window              | page 22-87                        |
|                                                                                      | LCK_EXP_WINDOW      | 304E0174h      | Lock Expiration Window             | page 22-88                        |
|                                                                                      | VIT_EXP_WINDOW      | 304E0178h      | Viterbi Expiration Window          | page 22-88                        |
|                                                                                      | SYNC_EXP_WINDOW     | 304E017Ch      | Sync Expiration Window             | page 22-88                        |
|                                                                                      | RS_EXP_WINDOW       | 304E0180h      | RS Expiration Window               | page 22-89                        |
|                                                                                      | TRI_STATE_CNTRL     | 304E0194h      | TRI-State Control                  | page 22-89                        |
|                                                                                      | DCII_CLK_CNTRL      | 304E0198h      | DCII Clock Control                 | page 22-90                        |
|                                                                                      | CLOCK_CONTROL       | 304E019Ch      | Clock Control                      | page 22-91                        |
| <b>DMA controller register names have the prefix of DMA_ and the suffix of _REG.</b> |                     |                |                                    |                                   |
|                                                                                      | DMA_CAPABILITY_REG  | 30500000h      | DMA Controller Capability Register | page 6-4                          |

**Table 6. CX24138 Register Index (17 of 20)**

| *                                                                                         | Register Name           | Address             | Description                                   | Refer to CX2414X Document 102210B |
|-------------------------------------------------------------------------------------------|-------------------------|---------------------|-----------------------------------------------|-----------------------------------|
|                                                                                           | DMA_MODE_REG            | 30500004h           | DMA Controller Mode Bits                      | page 6-4                          |
|                                                                                           | DMA_INT_REG             | 30500008h           | DMA Controller Interrupt Status Register (RO) | page 6-5                          |
|                                                                                           | DMA_REQSTAT_REG         | 3050000Ch           | DMA Request Status Register                   | page 6-5                          |
|                                                                                           | DVTIMER_COUNT           | 305000010           |                                               |                                   |
|                                                                                           | DVTIMER_LIMIT           | 305000014           |                                               |                                   |
|                                                                                           | DVTIMER_MODE            | 305000018           |                                               |                                   |
| <b>DMA Channel 0 Registers (these registers are replicated for each channel present)</b>  |                         |                     |                                               |                                   |
|                                                                                           | DMA_CH0_CTRL_REG        | 30500100h           | DMA Channel 0 Control Register                | page 6-6                          |
|                                                                                           | DMA_CH0_STAT_REG        | 30500104h           | DMA Channel 0 Status Register                 | page 6-8                          |
|                                                                                           | DMA_CH0_SRCADDR_REG     | 30500108h           | DMA Channel 0 Source Address                  | page 6-9                          |
|                                                                                           | DMA_CH0_DSTADDR_REG     | 3050010Ch           | DMA Channel 0 Destination Address             | page 6-9                          |
|                                                                                           | DMA_CH0_SRCBASE_REG     | 30500110h           | DMA Channel 0 Source Base Address             | page 6-9                          |
|                                                                                           | DMA_CH0_SRCBUF_REG      | 30500114h           | DMA Channel 0 Source Buffer Information       | page 6-10                         |
|                                                                                           | DMA_CH0_DSTBASE_REG     | 30500118h           | DMA Channel 0 Destination Base Address        | page 6-10                         |
|                                                                                           | DMA_CH0_DSTBUF_REG      | 3050011Ch           | DMA Channel Destination Buffer                | page 6-10                         |
|                                                                                           | DMA Channel 1 Registers | 30500120h-3050013Ch | DMA Registers for Channel 1                   | -                                 |
| <b>(If more than 2 DMA channels exist, their registers are mapped after channels 0-1)</b> |                         |                     |                                               |                                   |
|                                                                                           | DMA_STRIDE_CTL          | 305001E0            | DMA Stride Channel Control Register           | page 6-11                         |
|                                                                                           | DMA_STRIDE_STAT         | 305001E4            | DMA Stride Channel Status Register            | page 6-11                         |
|                                                                                           | DMA_STRIDE_SRCADDR      | 305001E8            | DMA Stride Channel Source Address             | page 6-12                         |
|                                                                                           | DMA_STRIDE_DSTADDR      | 305001EC            | DMA Stride Channel DEST. Address              | page 6-12                         |
|                                                                                           | DMA_STRIDE_SRCBASE      | 305001F0            | DMA Stride Channel Source Base                | page 6-12                         |
|                                                                                           | DMA_STRIDE_RUN          | 305001F4            | DMA Stride Channel Run length                 | page 6-13                         |
|                                                                                           | DMA_STRIDE_DSTBASE      | 305001F8            | DMA Stride Channel DEST. Base                 | page 6-13                         |
|                                                                                           | DMA_STRIDE_MSTRIDE      | 305001FC            | DMA Stride Channel Stride Register            | page 6-14                         |

**Table 6. CX24138 Register Index (18 of 20)**

| *                                                                                                                                        | Register Name   | Address              | Description                                                  | Refer to CX2414X Document 102210B |
|------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------------|--------------------------------------------------------------|-----------------------------------|
| <b>UART register names have the prefix of UART_ and the suffix of _REG. UART 1 base address is 30540000h, and UART 3 is at 305D0000h</b> |                 |                      |                                                              |                                   |
|                                                                                                                                          | FIFO            | 305x0000h            | BDS=0Write: Top of Transmit FIFORead: Bottom of Receive FIFO | page 7-19                         |
|                                                                                                                                          | BRDL            |                      | BDS=1Lower Baud Rate Divisor Register                        | page 7-20                         |
|                                                                                                                                          | IRQE            | 305x0004h            | BDS=0Interrupt Enable Register                               | page 7-21                         |
|                                                                                                                                          | BRDU            |                      | BDS=1Upper Baud Rate Divisor Register                        | page 7-22                         |
|                                                                                                                                          | FIFC            | 305x0008h            | FIFO Control Register                                        | page 7-23                         |
|                                                                                                                                          | FRMC            | 305x000Ch            | Frame Control Register                                       | page 7-24                         |
|                                                                                                                                          | STAT            | 305x0014h            | Status Register                                              | page 7-25                         |
|                                                                                                                                          | IRLVL           | 305x0018h            | Interrupt Level Register                                     | page 7-27                         |
| <b>Infra-Red Remote Control Interface</b>                                                                                                |                 |                      |                                                              |                                   |
| *                                                                                                                                        | CNTL            | 30560000h            | Control Register                                             | page 7-67                         |
|                                                                                                                                          | -               | 30560004h            | Reserved                                                     | -                                 |
|                                                                                                                                          | RXCLK           | 30560008h            | Receive Clock Divider Register                               | page 7-71                         |
|                                                                                                                                          | -               | 3056000Ch            | Reserved                                                     | -                                 |
| *                                                                                                                                        | STAT            | 30560010h            | Status Register                                              | page 7-73                         |
| *                                                                                                                                        | IRQEN           | 30560014h            | Interrupt Enable Register                                    | page 7-74                         |
| *                                                                                                                                        | FILTR           | 30560018h            | Low Pass Filter Register                                     | page 7-76                         |
| *                                                                                                                                        | FIFO            | 30560040h - 3056007C | Receive FIFO                                                 | page 7-78                         |
| <b>Audio Interface (305900xxh) – prefix: AUD_ suffix _REG</b>                                                                            |                 |                      |                                                              |                                   |
| *                                                                                                                                        | CHANNEL_CONTROL | 30590000h            | Channel control register                                     | page 11-10                        |
|                                                                                                                                          | PLAY_A_START    | 30590004h            | Play Back Buffer A Start Address register                    | page 11-11                        |
|                                                                                                                                          | PLAY_A_STOP     | 30590008h            | Play Back Buffer A Stop Address register                     | page 11-11                        |
|                                                                                                                                          | PLAY_B_START    | 3059000Ch            | Play Back Buffer B Start Address register                    | page 11-11                        |
|                                                                                                                                          | PLAY_B_STOP     | 30590010h            | Play Back Buffer B Stop Address register                     | page 11-11                        |
|                                                                                                                                          | PLAY_STATUS     | 30590014h            | Play Back Buffer Address Status register                     | page 11-11                        |
|                                                                                                                                          | PLAY_CONTROL    | 30590018h            | Play Back FIFO Control register                              | page 11-12                        |

**Table 6. CX24138 Register Index (19 of 20)**

| *                                                                                | Register Name           | Address   | Description                                     | Refer to CX2414X Document 102210B |
|----------------------------------------------------------------------------------|-------------------------|-----------|-------------------------------------------------|-----------------------------------|
|                                                                                  | CAPT_A_START            | 3059001Ch | Capture Buffer A Start Address register         | page 11-11                        |
|                                                                                  | CAPT_A_STOP             | 30590020h | Capture Buffer A Stop Address register          | page 11-11                        |
|                                                                                  | CAPT_B_START            | 30590024h | Capture Buffer B Start Address register         | page 11-11                        |
|                                                                                  | CAPT_B_STOP             | 30590028h | Capture Buffer B Stop Address register          | page 11-11                        |
|                                                                                  | CAPT_STATUS             | 3059002Ch | Capture Buffer Address Status register          | page 11-11                        |
|                                                                                  | CAPT_CONTROL            | 30590030h | Capture FIFO Control register                   | page 11-12                        |
|                                                                                  | OUTP_CONTROL            | 30590034h | Output Control register                         | page 11-13                        |
|                                                                                  | CLOCK_CONTROL           | 30590038h | Clock Control register                          | page 11-14                        |
|                                                                                  | FRAME_PROTOCOL          | 3059003Ch | Frame Protocol register                         | page 11-15                        |
|                                                                                  | NULL                    | 30590040h | Null Audio register                             | page 11-17                        |
|                                                                                  | LEFT_ATTEN              | 30590044h | Left Channel Audio Attenuation Value register   | page 11-17                        |
|                                                                                  | RIGHT_ATTEN             | 30590048h | Right Channel Audio Attenuation Value register  | page 11-17                        |
|                                                                                  | PLAY_INT_ADDR           | 3059004Ch | Play Back Interrupt Address Definition register | page 11-19                        |
|                                                                                  | CAPT_INT_ADDR           | 30590050h | Capture Interrupt Address Definition register   | page 11-19                        |
|                                                                                  | PLAY_INT_STAT           | 30590054h | Play Back Interrupt Status register             | page 11-19                        |
|                                                                                  | CAPT_INT_STAT           | 30590058h | Capture Interrupt Status register               | page 11-19                        |
|                                                                                  | SPDIF_PGM_CHAN_STAT     | 3059005Ch | SPDIF Programmable Channel Status Reg           |                                   |
| <b>Pulse Timer register names have the prefix of PT_ and the suffix of _REG.</b> |                         |           |                                                 |                                   |
|                                                                                  | CNTL                    | 305B0000h | Control Register                                | page 7-82                         |
|                                                                                  | FILTR                   | 305B0004h | Low Pass Filter Register                        | page 7-83                         |
|                                                                                  | CLKD                    | 305B0008h | Clock Divider Register                          | page 7-85                         |
|                                                                                  | STAT                    | 305B000Ch | Status Register                                 | page 7-86                         |
|                                                                                  | FIFO                    | 305B0010h | FIFO                                            | page 7-87                         |
|                                                                                  | I2C Interface 305E00xxh |           |                                                 |                                   |
|                                                                                  | I2C_MODE_REG            | 305E0000h | I2C Mode Register                               | page 7-1                          |
|                                                                                  | I2C_CTRL_REG            | 305E0004h | I 2C Control Register                           | page 7-2                          |
|                                                                                  | I2C_STAT_REG            | 305E0008h | I2C Status Register                             | page 7-3                          |

**Table 6. CX24138 Register Index (20 of 20)**

| * | Register Name | Address   | Description            | Refer to CX2414X Document 102210B |
|---|---------------|-----------|------------------------|-----------------------------------|
|   | I2C_RDATA_REG | 305E000Ch | I2C Read Data Register | page 7-4                          |

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## Comparison between CX24138 and CX2414X

### 3.1 Function Comparison

Because CX24138 is a reduction version of CX2414X, some functions are not supported in CX24138. [Table 7](#) compares the functions of CX24138 and CX2414X, indicating in the middle column whether or not any differences exist. Details on each listed function are described in *CX2414X Interactive TV Decoder IC Manual*, document 102210B. For those details, see the page listed in the “Refer to CX2414X Document 102210B” column.

**Table 7. Function Comparison between CX24138 and CX2414X (1 of 3)**

| Function name                        | Difference from CX2414X                                                                                                                                                                                                                                                                                                                                             | Refer to CX1414X Document 102210B |
|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| Memory Map                           | None.                                                                                                                                                                                                                                                                                                                                                               | page 3-1                          |
| System Register                      | None.                                                                                                                                                                                                                                                                                                                                                               | page 4-1                          |
| System Components                    | Some interrupts are not supported by CX24138, the register definitions of interrupt controller are different from CX2414X (refer to <a href="#">Section 3.2.1</a> of this CX24138 document).                                                                                                                                                                        | page 5-1                          |
| DMA Controller                       | None.                                                                                                                                                                                                                                                                                                                                                               | page 6-1                          |
| I2C Interface                        | There are two instances of the I2C interface in CX2414X. One is located at starting address 305E0000h and the second at 305E0100h. In CX24138, only reserves the I2C interface starting at 305E0000h.                                                                                                                                                               | page 7-1                          |
| General Purpose I/O Controller (PIO) | Because the CX24138 is a reduced version of CX2414X, many GPIO pins are not available. GPIO pins which are still available are listed in <a href="#">Table 22</a> of this CX24138 document. The corresponding bits in the PIO register can be set or reset to decide the function of individual corresponding GPIO pins, while those GPIOs not listed are reserved. | page 7-7                          |
| Uart                                 | In CX2414X, there are three UARTs: UART1 is located at base address 30540000h, UART2 is located at base address 30550000h and UART3 is located at base address 305D0000h. In CX24138, UART2 is not supported.                                                                                                                                                       | page 7-18                         |
| Smart Card Interface                 | CX24138 doesn't contain Smart Card Interface.                                                                                                                                                                                                                                                                                                                       | page 7-33                         |
| Infrared Remote Controller           | CX2414X contains three IR (Infrared Remote) Controller interfaces, each has transmitting and receiving functions. CX24138 only provides one IR interface, which is located at base address 30560000h and has only receiving function. The register definitions are also different from CX2414X (refer to <a href="#">Section 3.2.3</a> of this CX24138 document).   | page 7-64                         |
| Pulse Timer                          | None.                                                                                                                                                                                                                                                                                                                                                               | page 7-80                         |

**Table 7. Function Comparison between CX24138 and CX2414X (2 of 3)**

| Function name                        | Difference from CX2414X                                                                                                                                                                                                                                                             | Refer to CX2414X Document 102210B |
|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| Modem AFT                            | CX24138 doesn't provide Modem AFT function.                                                                                                                                                                                                                                         | page 7-89                         |
| SSD (SmartDAA System Side Device)    | CX24138 doesn't provide SSD.                                                                                                                                                                                                                                                        | page 7-96                         |
| Pulse Width Modulator                | None.                                                                                                                                                                                                                                                                               | page 7-106                        |
| External Bus Interface               | CX24138 doesn't contain PCI and ATA interface as in CX2414X, and the register definitions are also different from CX2414X (refer to <a href="#">Section 3.2.4</a> of this CX24138 document). In addition, the IO bus control signal IO_READY is erased; do not use this signal.     | page 8-1                          |
| GXA (Graphics Accelerator)           | None.                                                                                                                                                                                                                                                                               | page 9-1                          |
| DRM (Display Refresh Module)         | None.                                                                                                                                                                                                                                                                               | page 10-1                         |
| PCM Audio I/O Controller             | Doesn't support Dolby® Digital relative functions (refer to <a href="#">Section 3.2.6</a> of this CX24138 document).                                                                                                                                                                | page 11-1                         |
| DTDC (Digital TV Decoder Core)       | Doesn't support Dolby® Digital relative functions                                                                                                                                                                                                                                   | page 12-1                         |
| DTDC CPU Interface                   | Doesn't support Dolby® Digital relative functions (refer to <a href="#">Section 3.2.7</a> of this CX24138 document).                                                                                                                                                                | page 13-1                         |
| DTDC High Speed Data Port Controller | CX2414X provides a serial external demodulator port ED0, two serial/parallel high-speed data ports HSDP 0 and HSDP 1. CX24138 doesn't provide ED0 port, and only provides one serial high-speed data port HSDP 0 (refer to <a href="#">Section 3.2.2</a> of this CX24138 document). | page 14-1                         |
| DTDC MPEG System Parser              | None.                                                                                                                                                                                                                                                                               | page 15-1                         |
| DTDC Video Decoder                   | None.                                                                                                                                                                                                                                                                               | page 16-1                         |
| DTDC MPEG Audio Decoder              | Doesn't support Dolby® Digital relative functions.                                                                                                                                                                                                                                  | page 17-1                         |
| DTDC System Interactions             | Doesn't support Dolby® Digital relative functions.                                                                                                                                                                                                                                  | page 18-1                         |
| ARM920T Microprocessor               | None.                                                                                                                                                                                                                                                                               | page 19-1                         |
| Synchronous Memory Interface         | Because IO_CS4# is tied to 0, CX24138 only supports 16-bit SDRAM interface.                                                                                                                                                                                                         | page 20-1                         |
| Demodulator                          | None.                                                                                                                                                                                                                                                                               | page 22-1                         |
| TV Encoder                           | None.                                                                                                                                                                                                                                                                               | page 23-1                         |

**Table 7. Function Comparison between CX24138 and CX2414X (3 of 3)**

| Function name   | Difference from CX2414X | Refer to CX2414X Document 102210B |
|-----------------|-------------------------|-----------------------------------|
| Parametric Data | None.                   | page 24-1                         |

## 3.2 Register Definition and Table

Because some functions supported by CX2414X are not supported by CX24138, the corresponding register definitions and tables should be changed. All of the differences between the CX24138 and CX2414X register definitions and tables are listed from [Sections 3.2.1 to 3.2.7](#). Other register definitions and tables are the same, and are described in *CX2414X Interactive TV Decoder IC Manual*, document 102210B.

### 3.2.1 Interrupt Controller

[Table 8](#) lists the CX24138 top-level interrupt status positions bit contents. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 5-29.

**Table 8. Top-Level Interrupt Status Positions Bit Contents (1 of 2)**

| Bit | Name | Description                                                                                                                                                                                                                     | Refer to CX2414X Document 102210B               |
|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| 31  | TIM  | Timer Interrupts. This interrupt is not latched, it is automatically set when any timer IRQ status bit is set within the eight timers, and is cleared only when all bits within the timer IRQ register are cleared.             | "General Purpose Timers Registers" on page 5-36 |
| 30  | PIO  | General Purpose I/O Interrupts. This interrupt is not latched, it is automatically set when any PIO IRQ status bit is set within the PIO controller, and is cleared only when all bits within the PIO IRQ register are cleared. | Section 7.2.1                                   |
| 29  | PWM  | Pulse Width Modulator Interrupt. This interrupt is not latched, it is automatically set when either IRQ status bit is set within the PWM module, and is cleared only when both bits within the PWM IRQ register are cleared.    | Table 7-86                                      |
| 28  | PAR3 | Reserved.                                                                                                                                                                                                                       |                                                 |
| 27  | PAR2 | Reserved.                                                                                                                                                                                                                       |                                                 |
| 26  | -    | Reserved.                                                                                                                                                                                                                       |                                                 |
| 25  | -    | Reserved.                                                                                                                                                                                                                       |                                                 |
| 24  | GXA  | Graphics Accelerator Interrupt.                                                                                                                                                                                                 |                                                 |
| 23  | -    | Reserved.                                                                                                                                                                                                                       |                                                 |
| 22  | PAR0 | Programmable Parser 0 Interrupt.                                                                                                                                                                                                |                                                 |
| 21  | -    | Reserved.                                                                                                                                                                                                                       |                                                 |

**Table 8. Top-Level Interrupt Status Positions Bit Contents (2 of 2)**

| Bit | Name | Description                           | Refer to CX2414X Document 102210B |
|-----|------|---------------------------------------|-----------------------------------|
| 20  | CRYP | Cryptography Engine.                  |                                   |
| 19  | -    | Reserved.                             |                                   |
| 18  | -    | Reserved.                             |                                   |
| 17  | PT   | Pulse Timer Interrupt.                | Table 7-70                        |
| 16  | -    | Reserved                              |                                   |
| 15  | -    | Reserved                              |                                   |
| 14  | DMA  | DMA Controller Interrupt              | Table 6-5                         |
| 13  | -    | Reserved.                             |                                   |
| 12  | UT1  | UART 1 Interrupt.                     |                                   |
| 11  | -    | Reserved.                             |                                   |
| 10  | IR   | Infrared Remote Controller Interrupt. |                                   |
| 9   | DVT  | DV Timer.                             |                                   |
| 8   | ADT  | Audio Transmit Interrupt.             | Section 11.3                      |
| 7   | ADR  | Audio Receive Interrupt.              | Section 11.3                      |
| 6   | -    | Reserved.                             |                                   |
| 5   | -    | Reserved.                             |                                   |
| 4   | RTC  | Real Time Clock Interrupt.            |                                   |
| 3   | MPG  | MPEG Interrupt.                       | Table 13-9                        |
| 2   | DRM  | DRM Interrupt.                        | Table 10-10                       |
| 1   | -    | Reserved.                             |                                   |
| 0   | EXP  | Expansion interrupt register IRQ.     |                                   |

The CX24138 expansion positions bit contents is listed in [Table 9](#). For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 5-30.

**Table 9. Expansion Positions Bit Contents**

| Bit  | Name | Description                    |
|------|------|--------------------------------|
| 6-31 | RES  | Reserved.                      |
| 5    | -    | Reserved.                      |
| 4    | DMOD | Demodulator.                   |
| 3    | -    | Reserved.                      |
| 2    | I2C0 | Primary I2C controller #0.     |
| 1    | CMRX | ARM Communication Register RX. |
| 0    | CMTX | ARM Communication Register TX. |

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## 3.2.2 High-Speed Data Port

### HSDP0 Control Register

|              |                                                                                                                                                                                                                      |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | TSC_PORT_CNTL_REG                                                                                                                                                                                                    |
| Hex address: | 304CC008h, read/write                                                                                                                                                                                                |
| Size:        | 32 bits                                                                                                                                                                                                              |
| Function:    | The contents of the HSDP 0 control register is shown in <a href="#">Table 10</a> . For CX2414X, the corresponding table is located in <i>CX2414X Interactive TV Decoder IC Manual</i> , document 102210B Table 14-6. |

**Table 10. HSDP 0 Control Register Bit Definitions**

| Bit   | Function                                                                                                                                                                 |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | Reserved                                                                                                                                                                 |
| 26:24 | TSx Wrap Sub-select.<br>0 = Reserved.<br>1 = Internal Demod Serial Mode, TSB.<br>2-3 = Reserved.<br>4 = Internal Demod Parallel Mode, TSE data.<br>5-7 = Reserved.       |
| 23:22 | Reserved – write zeroes.                                                                                                                                                 |
| 21:20 | Port clocking mode.<br>11 = Reserved.<br>10 = Generate clock, see HSDP0 Clock Control register.<br>01 = Use HSDP_CLK PLL output.<br>00 = Clock is input.                 |
| 19:18 | Output data sub-select.<br>11 = Reserved.<br>10 = Reserved.<br>01 = Reserved.<br>00 = Programmable Parser 0.                                                             |
| 17:16 | Output data select.<br>11 = Reserved.<br>10 = Output FIFO disabled.<br>01 = TSx input data as selected by bit 26:24.<br>00 = Demux output data as selected by bit 19:18. |
| 15:14 | Reserved -- write zeroes.                                                                                                                                                |
| 13    | Output modes enable.<br>Must write to 0, then 1 in output modes. This acts as a outputlogic reset after the clock is configured.                                         |

**Table 10. HSDP 0 Control Register Bit Definitions**

| Bit   | Function                                                                                                    |
|-------|-------------------------------------------------------------------------------------------------------------|
| 12    | Serial Port mode enable.<br>1 = Serial input/output, enable serial to parallel conversion.<br>0 = Reserved. |
| 11:10 | Reserved – write zeroes.                                                                                    |
| 9:8   | Reserved – write zeroes.                                                                                    |
| 7:3   | Reserved – write zeroes.                                                                                    |
| 2     | Input Ignore fail.<br>0 = use fail signal.<br>1 = Ignore fail signal.                                       |
| 1     | Input Error/Fail signal polarity.<br>1 = Active Low.<br>0 = Active High.                                    |
| 0     | Clock polarity.<br>1 = Falling Edge.<br>0 = Rising Edge.                                                    |

**Demux Input Selection Register**

Name: SP\_INPUT\_CNTL\_REG

Hex address: 304CC020h

Size: Read/write 32 bits

Function: The contents of the Demux input selection register is shown in [Table 11](#). For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 14-9.

**Table 11. Demux Input Selection Register Bit Definitions**

| Bit  | Function                                                                                                                                                                                                                             |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | Reserved - write zeroes                                                                                                                                                                                                              |
| 2:0  | Programmable Parser 0 input selection.<br>111 = Reserved.<br>110 = Reserved.<br>101 = Reserved.<br>100 = Internal Demodulator Parallel.<br>011 = Reserved.<br>010 = HSDP 0.<br>001 = Internal Demodulator Serial.<br>000 = Reserved. |

**Table 11. Demux Input Selection Register Bit Definitions**

| Bit                                                                                                                        | Function |
|----------------------------------------------------------------------------------------------------------------------------|----------|
| <b>GENERAL NOTE:</b> After reset, the value in [2:0] is 000. It should be changed to 100, 010, or 001 by system boot code. |          |

**Transport Stream Packet Control Register**

|              |                                                                                                                                                                                                               |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | TS_PKT_CNTL_REG                                                                                                                                                                                               |
| Hex address: | 304CC040h, read/write                                                                                                                                                                                         |
| Size:        | 32 bits                                                                                                                                                                                                       |
| Function:    | The contents of the Transport Stream packet control register is shown in Table 12. For CX2414X, the corresponding table is located in CX2414X Interactive TV Decoder IC Manual, document 102210B Table 14-11. |

**Table 12. Transport Stream Packet Control Register Bit Definitions**

| Bit   | Function                                                                                                                                                                                |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | Reserved – write zeroes.                                                                                                                                                                |
| 26    | Packet FIFO enable. Provides data rate matching to avoid data gaps (via clockgaps or valid gaps) in packet output.<br>1 = Packet FIFO enabled.<br>0 = Packet FIFO disabled.             |
| 25    | Error signal function for bad packets. 1 = Hold error for entire packet<br>0 = Assert error with sync byte only.                                                                        |
| 24    | DSS packet mode. Bit 7 of Byte 0 of the 130 byte DSS packet, should toggle for each packet sent to an output port. This is checked and sync information is provided back to the parser. |
| 23    | Reserved – write zeroes.                                                                                                                                                                |
| 22:18 | Output FIFO threshold. Number of words required in output FIFO before data will start to flow to HSDP.                                                                                  |
| 17:16 | Reserved – write zeroes.                                                                                                                                                                |
| 15:8  | Sync byte code. Reset value = 0x47 (ignored in DSS mode).                                                                                                                               |
| 7:0   | Packet size. Reset value = 188. Set to 130 for DSS mode.                                                                                                                                |

### Transport Stream Error Status Register

Name: TS\_ERR\_STATUS\_REG

Hex address: 304CC048h, read/write 32

Size: 32 bits

Function: The contents of the Transport Stream Error below. Refer to [Table 13](#). Writing 1s clears the respective bits. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 14-12.

**Table 13. Transport Stream Error Status Register Bit Definitions**

| Bit   | Function                                                                                                         |
|-------|------------------------------------------------------------------------------------------------------------------|
| 31:10 | Reserved – write zeroes.                                                                                         |
| 9     | Reserved – write zeros.                                                                                          |
| 8     | Reserved – write zeros.                                                                                          |
| 7:2   | Reserved – write zeroes.                                                                                         |
| 1     | Port 0 output overrun.                                                                                           |
| 0     | Lost sync on HSDP 0 output (expected sync byte does not equal TS_PKT_CNTL[15:8] or fails to toggle in DSS mode). |

### HSDP 0 Clock Control Register

Name: TSC\_GEN\_CLK\_CNTL\_REG

Hex address: 304CC058, read/write

Size: 32 bits

Function: The contents of the HSDP 0 Clock control register is shown below. Refer to [Table 14](#). The clock count values are the number of HSDPCLK clock cycles desired -1. Typically the HSDPCLK is set to 108 MHz. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 14-13.

**Table 14. HSDP 0 Clock Control Register Bit Definitions**

| Bit   | Function                                                                                                        |
|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved – write zeroes.                                                                                        |
| 15:8  | Total clock count. Programmable Parser clock (HSDPCLK) divided by this value. Minimum allowed value is 2.       |
| 7:0   | Clock high count. Minimum allowed value is 1. This value must be at least 1 less than Total clock count [15:8]. |

### 3.2.3 Infrared Remote Control Interface

#### Control Register

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | IR_CNTL_REG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Hex address: | 30560000h, read/write                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Size:        | 32 Bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Function:    | The control register contains nine bit-fields which control various aspects of the IR port's receive data streams. Features which are controlled using this register include, Rx Fifo load on timer overflow, loop back operation, carrier polarity, FIFO service request levels, enabling/ disabling the IR port's receiver, enabling/disabling the RX FIFOs, selection of carrier modulation and demodulation, control of which type of edge to start and stop the pulse timer for demodulated receive data, and control of a window which is used to predict when the next receive carrier transition is expected. |

When changing any configuration in this register, always disable the IR's receiver first, then reprogram the mode of operation and enable the receiver. This register is reset to all zeros.

Table 15 lists the CX24138 IR control bit descriptions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 7-62.

**Table 15. IR Control Bit Descriptions (1 of 2)**

| Bit   | Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | -    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 14    | R    | Receive Fifo load on Timer Overflow Disable.<br>0 = Load Rx Fifo with l's and Rx_data_lh level on timer overflow;<br>1 = Do Not load Rx fifo on timer overflow.                                                                                                                                                                                                                                                                                                                                                     |
| 13    | LBM  | Loop Back Mode.<br>Must be 0 to make receive operation functions normally via the IR port's pins.                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 12    | CPL  | Carrier Polarity.<br>0 = If mod/demodulation enabled, ones received as series of carrier transitions (mark), zeros received as the absence of a carrier or no transitions (space). If mod/demodulation disabled, ones received as logic high, zeros as logic low.<br>1 = If mod/demodulation enabled, ones received as the absence of a carrier or no transitions (space), zeros received as a series of carrier transitions (mark). If mod/demodulation disabled, ones received as logic low, zeros as logic high. |
| 11    | ---- | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 15. IR Control Bit Descriptions (2 of 2)**

| Bit | Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | RIC  | Receiver Interrupt Control.<br>0 = Receive FIFO service interrupt/DMA request asserted when RX FIFO is half full or greater, negated when RX FIFO is less than half full.<br>1 = Receive FIFO service interrupt/DMA request asserted when RX FIFO is not empty, negated when RX FIFO is empty.(see status register below for a description of this irq).                                                                                                                                                                                   |
| 9   | ---  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8   | RXE  | Receiver Enable.<br>0 = Disable receiver.<br>1 = Enable receiver.                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 7   | ---  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 6   | RFE  | Receive FIFO Enable.<br>0 = Disable and reset receive FIFO to all zeroes.<br>1 = Enable receive FIFO.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5   | ---  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 4   | DMD  | Receive Demodulation Enable.<br>0 = Disable receive carrier demodulation, receive data as simple logic levels.<br>1 = Enable receive carrier demodulation, detect a mark as a series of RX pin transitions, and a space as the absence of transitions.<br>Programming the carrier polarity bit determines whether marks/high or spaces/low are decoded as ones or zeroes.                                                                                                                                                                  |
| 3:2 | EDG  | Receive Edge Detect Control.<br>00 = Disabled.<br>01 = Falling edges trigger RX filter/pulse timer start/stop.<br>10 = Rising edges trigger RX filter/pulse timer start/stop.<br>11 = Either edge trigger RX filter/pulse timer start/stop.<br>The RX low pass filter and pulse width timer starts/ends a pulse duration measurement each time the programmed edge on the demodulated input is detected.                                                                                                                                   |
| 1:0 | WIN  | Next Predicted Receive Carrier Edge Window Limits.<br>00 = Next carrier edge predicted to be 16 RX clocks -3/+3.<br>01 = Next carrier edge predicted to be 16 RX clocks -4/+3.<br>10 = Next carrier edge predicted to be 16 RX clocks -3/+4.<br>11 = Next carrier edge predicted to be 16 RX clocks -4/+4.<br>Once the first rising-edge within a carrier burst is detected, each subsequent rising-edge should occur 16 RX clock cycles later, plus or minus the programmed limits above, transitions out of this range are not detected. |

**Status Register**

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | IR_STAT_REG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Hex address: | 30560010h, read-only                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Size:        | 32 Bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Function:    | The IR port's status register contains four status bits; three which can interrupt the CPU and two which can be polled. Bits 4, 1, and 0 are set and cleared automatically by hardware and signal when a hardware condition exists which must be handled by software. Any one of these three status bits produces an interrupt when set and its corresponding interrupt enable bit is set. Interrupt enable bits do not affect the setting and clearing of status bits. The receive busy flags are also set and cleared automatically by hardware (bits 2 and 3), but do not produce interrupts. They are polled by software to query whether the IR port is currently receiving IR data. In addition to interrupting the CPU, bit 4 can also trigger service requests to the DMA controller. The Interrupt Enable Register (IR_IRQEN_REG) is programmed to enable/disable the receive FIFO service requests to signal interrupts to the interrupt controller, and the DMA controller is programmed separately to respond to the FIFO service requests. This register is read-only, writes have no effect. |

Table 16 lists the CX24138 status bit descriptions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 7-66.

**Table 16. Status Bit Descriptions**

| Bit  | Name | Description                                                                                                                                                                                                                                                                                                               |
|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | -    | Reserved.                                                                                                                                                                                                                                                                                                                 |
| 5    | -    | Reserved.                                                                                                                                                                                                                                                                                                                 |
| 4    | RSR  | Receive FIFO Service Request.<br>0 = If RIC=0 in IR_CNTL_REG, receive FIFO is less than half full. If RIC=1, receive FIFO is empty.<br>1 = If RIC=0, receive FIFO is half full or more. If RIC=1, receive FIFO is not empty.<br>Generate a DMA request and an irq request if the RSE mask bit is set in the IR_IRQEN_REG. |
| 3    | -    | Reserved.                                                                                                                                                                                                                                                                                                                 |
| 2    | RBY  | Receiver Busy (non-interruptible).<br>0 = Receiver is idle.<br>1 = Receiver is busy.                                                                                                                                                                                                                                      |

**Table 16. Status Bit Descriptions**

| Bit | Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | ROR  | <p>Receive FIFO Overrun.</p> <p>0 = Receive FIFO contains one or more empty entries or is full but has not experienced an overrun.</p> <p>1 = Receive FIFO has experienced an overrun, generate an irq request if the ROE mask bit is set in the IR_IRQEN_REG.</p> <p><b>NOTE:</b> When an overrun occurs, data within the FIFO remains intact, and any new data from the RX pulse width counter is lost until the FIFO once again contains one or more empty entries.</p> |
| 0   | RTO  | <p>Receive Pulse Width Timer Time-out.</p> <p>0 = Receive pulse width counter has not reached its limit.</p> <p>1 = Receive pulse width counter has reached it's limit (contains all ones), generate an irq request if the RTE mask bit is set in the IR_IRQEN_REG.</p>                                                                                                                                                                                                    |

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**Interrupt Enable Register**

Name: IR\_IRQEN\_REG

Hex address: 30560014h, read/write

Size: 32 Bits

Function: The Interrupt Enable Register contains three bits which are used to mask or enable individual interrupt requests. Refer to the IR Status Register (IR\_STAT\_REG) for a description of each interrupt source. The interrupt enable bits do not effect the setting and clearing of the interrupt status bits. Each enable bit is logically ANDed with its corresponding status bit, and the resultant signals are all logically ORed to produce a single interrupt request to the interrupt controller.

Table 17 lists the CX24138 interrupt enable register bit descriptions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 7-67.

**Table 17. Interrupt Enable Register Bit Descriptions**

| Bit  | Name | Description                                                                                                                                                                     |
|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | -    | Reserved.                                                                                                                                                                       |
| 5    | -    | Reserved.                                                                                                                                                                       |
| 4    | RSE  | Receive FIFO Service Request Interrupt Enable.<br>0 = Receive FIFO interrupt disabled.<br>1 = Receive FIFO interrupt enabled.                                                   |
| 3:2  | -    | Reserved.                                                                                                                                                                       |
| 1    | ROE  | Receive FIFO Overrun Interrupt Enable.<br>0 = Receive FIFO overrun interrupt disabled.<br>1 = Receive FIFO overrun interrupt enabled.                                           |
| 0    | RTE  | Receive Pulse Width Timer Time-out Interrupt Enable.<br>0 = Receive pulse width timer time-out interrupt disabled.<br>1 = Receive pulse width timer time-out interrupt enabled. |

**FIFO Register**

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | IR_FIFO_REG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Hex address: | 30560040-7Ch, read/write                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Size:        | 32 Bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Function:    | The FIFO register provides access to the IR port's receive FIFOs. This register can be accessed by reading/writing any address from 30560040h to 3056007Ch. This address range allows the ARM load/store multiple instructions to be used to empty/fill the FIFOs. Reads of this register access the bottom of the receive FIFO, allowing incoming pulse width measurements to be removed. The receive FIFO is 18-bits wide x 8-entries deep. Bits 15-0 contain the pulse width measurement from the RX pulse width counter, bit 16 contains the state of the ir_in pin at the end of the measurement, and bit 17 is a tag which indicates whether more valid data is present within the FIFO. When the DMA controller is used to service the RX FIFOs, if RIC=0 in the IR_CNTL_REG, the burst size should be set at four words in each case. If RIC=1, the burst size should be set for one word. |

Table 18 lists the CX24138 FIFO register bit-field descriptions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 7-69.

**Table 18. FIFO Register Bit-Field Descriptions**

| Bit   | Name    | Description                                                                                                                          |
|-------|---------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | -       | Reserved                                                                                                                             |
| 17    | RX NDV  | Receive Next Data Valid (read-only).<br>0 = No more data in the RX FIFO.<br>1 = One or more entries of valid data remain in RX FIFO. |
| 16    | RX LVL  | Receive Pin Level.<br>Read: Value of demodulated input at end of RX pulse width measurement.                                         |
| 15:0  | RX FIFO | Receive Pulse Width Count/Measurement Value.<br>Read: Bottom entry of the receive FIFO.                                              |

## 3.2.4 I/O Interface Register Descriptions

### ROM Descriptor 0 Register

Name: ROM\_DESC0\_REG

Hex address: 30010000h, read/write

Size: 32-bit register

Function: Interface for ROM devices.

Table 19 lists the CX24138 ROM descriptor 0 register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 8-2.

**Table 19. ROM Descriptor 0 Register Bit Definitions**

| Bit                                                                                                               | Name                    | Description                                                                                                                                                                                                                    |
|-------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31                                                                                                                | DESC_TYPE               | 0 = The descriptor is a ROM descriptor.<br>1 = No ROM present.                                                                                                                                                                 |
| 30:24                                                                                                             | WR_WAIT <sup>(1)</sup>  | Access time in memory clock cycles for write operations.                                                                                                                                                                       |
| 23                                                                                                                | PROGRAM_FLASH           | Set to 1 when programming a bank of flash through this descriptor.                                                                                                                                                             |
| 22:16                                                                                                             | RD_WAIT <sup>(1)</sup>  | Access time in memory clock cycles for read operations.                                                                                                                                                                        |
| 15:12                                                                                                             | BST_WAIT <sup>(1)</sup> | Access time in memory clock cycles for page-mode operations.                                                                                                                                                                   |
| 11                                                                                                                | BST_ENBL                | Burst read timing enable (Page mode enable).                                                                                                                                                                                   |
| 10:8                                                                                                              | CHIP_SEL                | Encoded chip select to drive for this descriptor, NO CS2#, so cannot be config to 010.<br>000: IO_CS0 enabled.<br>001: IO_CS1 enabled.<br>010: Reserved.<br>011: IO_CS3 enabled.<br>100: IO_CS4 enabled.<br>101-111: Reserved. |
| 7:6                                                                                                               |                         | Reserved.                                                                                                                                                                                                                      |
| 5:4                                                                                                               | WIDTH                   | 00 = Reserved.<br>01 = 8-bit ROM attached.<br>10 = 16-bit ROM attached.<br>11 = Reserved.                                                                                                                                      |
| 3:0                                                                                                               |                         | Reserved.                                                                                                                                                                                                                      |
| <b>FOOTNOTE:</b><br><sup>(1)</sup> One clock cycle is added to the value internally to allow for I/O propagation. |                         |                                                                                                                                                                                                                                |

**ROM Descriptor 1-3 Register**

|             |                                                                                                                                                                                           |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name        | ROM_DESC[13]_REG                                                                                                                                                                          |
| Hex address | 30010000h -3001000C, read/write                                                                                                                                                           |
| Size        | 32-bit register                                                                                                                                                                           |
| Function    | Interface for either ROM or ISA devices. To program as a ROM device, refer to Table 3-11 (Table 8-2 in CX2414X). To program as an ISA device, refer to Table 3-12 (Table 8-3 in CX2414X). |

**ISA Descriptor 4-7 Registers**

|             |                                    |
|-------------|------------------------------------|
| Name        | ISA_DESC[47]_REG                   |
| Hex address | 30010010h to 3001001Ch, read/write |
| Size        | 4 32-bit registers                 |
| Function    | Interface for ISA devices          |

Table 20 lists the CX24138 ISA descriptor 4 through 7 register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 8-3.

**Table 20. ISA Descriptor 4 through 7 Register Bit Definitions**

| Bit                                                                                                               | Name                   | Description                                                                                                                            |
|-------------------------------------------------------------------------------------------------------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31                                                                                                                | DESC_TYPE              | 1 indicates the descriptor is an ISA descriptor.                                                                                       |
| 30:24                                                                                                             | WR_WAIT <sup>(1)</sup> | Access time in memory clock cycles for write operations.                                                                               |
| 23                                                                                                                |                        | Reserved.                                                                                                                              |
| 22:16                                                                                                             | RD_WAIT <sup>(1)</sup> | Access time in memory clock cycles for read operations.                                                                                |
| 15                                                                                                                | -                      | Reserved.                                                                                                                              |
| 14                                                                                                                | SYNC_IO                | Enable Synchronous I/O mode. All I/O from this descriptor is synchronized with respect to clock on CS3#.                               |
| 13:11                                                                                                             |                        | Reserved.                                                                                                                              |
| 10:8                                                                                                              | CHIP_SEL               | Encoded chip select to drive for this descriptor, NO CS2#, so cannot be config to 010.                                                 |
| 7                                                                                                                 | REG                    | Indicates the access requires the assertion of the isa_reg_ signal.                                                                    |
| 6                                                                                                                 | IO                     | 0 = Use IO_MEMRD#/IO_MEMWR# for accesses<br>1 = disable IO_MEMRD#/IO_MEMWR#.                                                           |
| 5:4                                                                                                               | WIDTH                  | 00 = 32-bit ROM attached (non-burst).<br>01 = 8-bit ROM attached<br>10 = 16-bit ROM attached.<br>11 = 32-bit ROM attached (non-burst). |
| 3:0                                                                                                               |                        | Reserved.                                                                                                                              |
| <b>FOOTNOTE:</b><br><sup>(1)</sup> One clock cycle is added to the value internally to allow for I/O propagation. |                        |                                                                                                                                        |

**ROM Mode Register**

Name: ROM\_MODE\_REG (Reserved)

Hex address: 30010030h, read/write

Size: 32-bit registers

Function Controls ROM interface operating modes

**Table 21** lists the ROM mode register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 8-6. Bits 11:8 control whether CS3# is used as a chip select or a clock for pseudo synchronous I/O operation. When set to 0, CS3# acts as a normal chip select. When set to a non-zero value, it becomes a clock derived from memclk that may be used with descriptors that have the SYNC\_IO bit set.

Name: ROM\_MODE\_REG (Reserved) Hex address: 30010030h, read/write Size: 32-bit registers Function: This register controls ROM interface operating modes.

**Table 21. ROM Mode Register Bit Definitions**

| Bit   | Name                  | Description                                                                                                                |
|-------|-----------------------|----------------------------------------------------------------------------------------------------------------------------|
| 31:12 |                       | Reserved.                                                                                                                  |
| 11:8  | SYNCRONOUS I/O ENABLE | 0 = Asynchronous I/O (normal operation).<br>1 = Reserved.<br>2-15 = Clock divider from the memory clock for the I/O clock. |
| 5:0   |                       | Reserved.                                                                                                                  |

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## 3.2.5 GPIO

Because the CX24138 is a reduced version of CX2414X, many GPIO pins are not available. GPIO pins which are still available are listed in [Table 22](#). The corresponding bits in the PIO register can be set or reset to decide the function of the individual corresponding GPIO pins. GPIOs not listed are reserved.

**Table 22. Available GPIO Pins (1 of 2)**

| Pin Name               | Corresponding PIO Register Bit |
|------------------------|--------------------------------|
| PIO001_UART1TX         | 1                              |
| PIO002_UART1RX         | 2                              |
| PIO005_IOA16           | 5                              |
| PIO006_IOA17           | 6                              |
| PIO007_IOA18           | 7                              |
| PIO012_IRIN1           | 12                             |
| PIO014_UART3TX_ED0VAL  | 14                             |
| PIO015_UART3TX_ED0SYNC | 15                             |
| PIO018_DCLKP           | 18                             |
| PIO024_PWM             | 24                             |
| PIO027_UHF             | 27                             |
| PIO029_HS1CLK          | 29                             |
| PIO030_HS1D0           | 30                             |
| PIO039_AUDSPDIF_CLK0   | 39                             |
| PIO041_AUDDEEMP_LRS    | 41                             |
| PIO042_AUDBITCK_CLF    | 42                             |
| PIO044_HS1RW           | 44                             |
| PIO045_HS0RW           | 45                             |
| PIO047_HS0D0           | 47                             |
| PIO055_HS0CLK          | 55                             |
| PIO056_HS0VALEN        | 56                             |
| PIO057_HS0SYNC         | 57                             |
| PIO062_HS0ERRAV_HDREQ  | 62                             |
| PIO063_IOA19           | 63                             |

**Table 22. Available GPIO Pins (2 of 2)**

| Pin Name             | Corresponding PIO Register Bit |
|----------------------|--------------------------------|
| PIO064_IOA20         | 64                             |
| PIO065_IOA21         | 65                             |
| PIO102_DDR           | 102                            |
| PIO106_DSPKR_XTALCLK | 106                            |
| PIO107_UCLK0         | 107                            |

## 3.2.6 PCM Audio I/O Controller

### Channel Control Register

|              |                                                                                                                                                                                                                                                                                                   |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name:        | AUD_CHANNEL_CONTROL_REG                                                                                                                                                                                                                                                                           |
| Hex address: | 30590000h, read/write                                                                                                                                                                                                                                                                             |
| Size:        | 32-bit register                                                                                                                                                                                                                                                                                   |
| Function:    | The channel control register contains bits which control major modes of operation including the enabling and disabling of both parallel and serial data paths. The contents of the channel control register can be updated at any time, allowing mode changes while the PCM Controller is active. |

Table 23 lists the channel control register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 11-5.

**Table 23. Channel Control Register Bit Definitions (1 of 2)**

| Bit  | Function                                                                                                                                                                                                                                                                                                                          |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | Transmit Normalization Bypass (optional).<br>Disables normalization or shifting of PCM data from playback FIFO prior to serialization that causes bits [19:0] to be properly aligned with the programmed output data size.<br>1 = Disable normalization.<br>0 = 20 bit normalization enabled.                                     |
| 30   | Receive Normalization Bypass (optional).<br>Disables normalization or shifting of PCM data to capture FIFO after parallelization that causes the MSBs of the programmed input data size to be shifted to align with bit [19:0] when saved to the capture FIFO.<br>1 = Disable normalization.<br>0 = 20 bit normalization enabled. |
| 29:6 | Reserved – write zeroes.                                                                                                                                                                                                                                                                                                          |

**Table 23. Channel Control Register Bit Definitions (2 of 2)**

| Bit | Function                                                                                                                                                                                                                                                                                                      |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | Audio Decoder PCM Pass-Through (optional).<br>Enables unattenuated serial PCM pass-through from the audio decoder out to a separate pin (not on same pin used for serial PCM from the playback FIFO) bypassing the capture and playback data paths.<br>1 = Enable audio decoder pass-through.<br>0 = Disable. |
| 4   | Reserved – write zeros.                                                                                                                                                                                                                                                                                       |
| 3   | Audio Decoder Serial PCM Input Attenuation Enable (optional).<br>1 = Serial PCM input from audio decoder attenuated before entering capture FIFO.<br>0 = Unattenuated.                                                                                                                                        |
| 2   | Serial Input/Output Enable.<br>Enables serial pin input/output (playback and capture serial data paths).<br>1 = Enabled.<br>0 = Disabled.                                                                                                                                                                     |
| 1   | Capture Enable.<br>Enables the audio input stream parallel data path (capture FIFO and buffers).<br>1 = Enabled.<br>0 = Disabled.                                                                                                                                                                             |
| 0   | Playback Enable.<br>Enables the audio output stream parallel data path (playback FIFO and buffers).<br>1 = Enabled.<br>0 = Disabled.                                                                                                                                                                          |

Table 24 lists the audio interface pin descriptions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 11-21.

**Table 24. Audio Interface Register Pin Descriptions (1 of 2)**

| Port Name             | I/O | Description                                                                                                                                                                                                                                                                                |
|-----------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AUD_DOUT_LR           | 0   | Left/Right PCM Data Output.<br>The aud_dout output contains multiplexed left and right channel PCM data. The channel is indicated by aud_lrck.                                                                                                                                             |
| PI0042_AUDBITCK_K_CLF | 0   | Serial PCM Bit Clock Output.<br>The audbitck output is either 32 or 64 times the sample frequency and indicates when serial PCM output data changes and is valid. aud_dout data changes on the falling edge of audbitck and is sampled by off-chip devices on the rising-edge of audbitck. |
| AUD_LRCK              | 0   | Audio Sample Rate Left/Right Clock Output.<br>The aud_lrck output changes at the sample frequency and indicates which channel (left or right) is currently being transmitted.                                                                                                              |
| PI0039_AUDSPDIF_CLK0  | 0   | SPDIF (IEC958) Output.<br>This audspdif output transmits serial SPDIF data and is selectable between two-channel PCM.                                                                                                                                                                      |

**Table 24. Audio Interface Register Pin Descriptions (2 of 2)**

| Port Name               | I/O | Description                                                                                                                                                                                                               |
|-------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PI0041_AUDDEE<br>MP_LRS | 0   | MPEG De-emphasis Output.<br>The auddeemp output is asserted if the selected de-emphasis standard is active.                                                                                                               |
| AUD_OSC1                | 0   | Audio Oversampling Clock Output1.<br>The aud_osc1 output is a clock, which is between 32 to 512 times the sample rate frequency and is used by off-chip devices which receive serial PCM data as their main clock source. |

## 3.2.7 DTDC CPU Interface

### Control 1 Register

Name: MPG\_CONTROL1\_REG

Hex address: 30400004h, read/write

Size: 32 bits

Function: MPG\_CONTROL1\_REG is used for configuring the audio decoder and the audio output controller.

Table 25 lists the CONTROL1 register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 13-9.

**Table 25. CONTROL1 Register Bit Definitions (1 of 3)**

| Bit   | Function                                                                                                                                                                                                                                                 |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | Enable Audio decode.<br>0 = Audio decode disabled.<br>1 = Audio decode is enabled when Audio Encoded buffer contains data.                                                                                                                               |
| 30    | Enable Video decode.<br>0 = Video decode disabled.<br>1 = Video decode is enabled when Video Encoded buffer contains data.                                                                                                                               |
| 29-28 | FSCODE – Audio sample frequency. Writable by software to inform spdif logic of Audio sample frequency when spdif PCM source is PCM Audio I/O Controller and audio decoder is disabled.<br>00 = 48kHz.<br>01 = 44.1kHz.<br>10 = 32 kHz.<br>11 = Reserved. |
| 27    | Select spdif PCM source.<br>0 = Audio Output Controller.<br>1 = PCM Audio I/O Controller.                                                                                                                                                                |

**Table 25. CONTROL1 Register Bit Definitions (2 of 3)**

| Bit     | Function                                                                                                                                                                                   |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26      | DIRECTV MODE.<br>1 = DIRECTV.<br>0 = DVB.                                                                                                                                                  |
| 25      | Enable Audio synchronization using audio PTS values.<br>0 = Audio decoded without PTS checks.<br>1 = Enable synchronization of Audio with transport stream PTS values.                     |
| 24      | Enable Audio context change.<br>0 = Normal transport stream context changes.<br>1 = Immediate context change is enabled. Used when audio stream is feed from software.                     |
| 23-21   | FSCODE – Audio sample frequency. Read Only.<br>000 = 48 KHz.<br>001 = 44.1 KHz.<br>010 = 32 KHz.<br>011 = Reserved '100' - 24 KHz.<br>101 = 22.05 KHz.<br>110 = 16 KHz.<br>111 = Reserved. |
| 20 - 19 | Select Audio Output Controller spdif PCM source.<br>00 = L/R data to spdif output<br>01 = Reserved<br>10 = Reserved<br>11 = Reserved                                                       |
| 18      | Audio Frame Start<br>Start audio start (for audio only mode). Active high.                                                                                                                 |
| 17 - 16 | Dual-Mono Reproduction Mode.<br>00 = Normal L/R.<br>01 = L data repeated on L/R.<br>10 = R data repeated on L/R.<br>11 = Reserved.                                                         |
| 15      | Audio Output Controller serial output format.<br>0 = I2S.<br>1 = Left-justified.                                                                                                           |
| 14      | Mute.<br>When 1, decoder PCM data will be muted regardless of audio decoding.                                                                                                              |
| 13      | Reserved.                                                                                                                                                                                  |
| 12      | IEC958_ professional.<br>0 = spdif output is consumer format.<br>1 = spdif output is professional format.                                                                                  |
| 11      | Reserved.                                                                                                                                                                                  |

**Table 25. CONTROL1 Register Bit Definitions (3 of 3)**

| Bit | Function                                                                              |
|-----|---------------------------------------------------------------------------------------|
| 10  | Halt decoding.<br>When 1, decoder will stop decoding and send acknowledge to DSR[13]. |
| 9:0 | Reserved.                                                                             |

**Decoder Status Register**

Name: MPG\_DECODE\_STATUS\_REG

Hex address: 3040001Ch, read only

Size: 32 bits

Function: MPG\_DECODE\_STATUS\_REG provides information on availability of bitstream data and on bitstream errors. This register has mixed access from the host. Access for each bit is defined in Table 26. R/W means read and write access. R indicates read only access and RC means read access with clear of these bits after the read is complete.

Table 26 lists the decoder status register bit definitions. For CX2414X, the corresponding table is located in *CX2414X Interactive TV Decoder IC Manual*, document 102210B Table 13-14.

**Table 26. Decoder Status Register Bit Definitions (1 of 2)**

| Bit   | Access | Description                                                                                                    |
|-------|--------|----------------------------------------------------------------------------------------------------------------|
| 31:21 | R/W    | Mailbox-used to pass information from Host to DSP.                                                             |
| 20    | R/W    | Should be Asserted to select decode of primary audio (MPEG audio).                                             |
| 19:15 | R      | Mailbox-used to pass information from DSP to Host.                                                             |
| 14    | R/W    | Audio Test.                                                                                                    |
| 13    | R      | Audio Test.                                                                                                    |
| 12    | RC     | Audio Bitstream Error Interrupt.<br>Cleared on read of DSR.                                                    |
| 11    | RC     | Audio Bitstream Error Interrupt.<br>Cleared on read of DSR.                                                    |
| 10:6  | RC     | Video Bitstream Error Interrupt (Error codes are listed in Table 13-15 of CX2414X).<br>Cleared on read of DSR. |
| 5     | RC     | Audio Bitstream Error Interrupt.<br>Cleared on read of DSR.                                                    |
| 4     | R      | Anc data is available.                                                                                         |
| 3     | R      | User data is available.                                                                                        |

**Table 26. Decoder Status Register Bit Definitions (2 of 2)**

| Bit | Access | Description                                                                       |
|-----|--------|-----------------------------------------------------------------------------------|
| 2-1 | RC     | Audio Bitstream Error Interrupt.<br>Cleared on read of DSR.                       |
| 0   | R      | New Host Command available.<br>Cleared when main controller receives the command. |

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